

Questa 6.5 Series Product Comparison			
Feature	ModelSim SE	Questa SV	Questa AFV
	Large Block/System Simulation	Advanced Verification, SystemVerilog	Advanced Verification, All Languages
<b>General</b>			
Licensing - Floating License	■	■	■
Language Neutral License	Option	N/A	N/A
ASIC Sign-Off	■	■	■
Platform-Independent Compiled Database	■	■	■
Native-Compiled Architecture	■	■	■
Incremental Compilation	■	■	■
32/64-Bit Cross-Compatibility	■	■	■
<b>Languages</b>			
SystemVerilog IEEE1800 Design	■	■	■
SystemVerilog IEEE1800 Verification	■	■	■
VHDL	■	■	■
Verilog	■	■	■
SystemC 2.2 IEEE 1666/OSCI 2.2	Option	Option	■
Mixed Language	Option	■	■
PSL IEEE 1850	■	■	■
Unified Power Format	■	■	■
Analog/Mixed Signal (Questa AMS Product)	Option	Option	Option
<b>Advanced Verification</b>			
Assertion-Based Verification	■	■	■
Questa Verification Library (Assertion Checker & Monitor Library)	■	■	■
Constrained-Random Test Generation	■	■	■
Open Verification Methodology (OVM)	■	■	■
Codelink (Processor-Based Verification)	■	Option	Option
Multi-View Verification Components (Verification IP Library)	■	Option	Option
<b>Verification Management &amp; Coverage</b>			
Code Coverage (with Toggle Coverage)	■	■	■
Functional Coverage	■	■	■
Unified Coverage DataBase (UCDB)	Code Coverage Only	■	■
Coverage Viewer	Code Coverage Only	■	■
Test Ranking	Code Coverage Only	■	■
Test Plan Tracking	■	■	■
<b>Design Entry, Debug, and Analysis</b>			
HDL Editor	■	■	■
Integrated Project Manager	■	■	■
Source Code Templates and Wizards	■	■	■
Interactive & Post-Simulation Debug	■	■	■
Dataflow Graphical & Textual Causality Traceback	■	■	■
FSM Debug	■	■	■
Source Annotation	■	■	■
Hyperlinked Navigation	■	■	■
Class Browser	■	■	■
Dynamic Thread Debug & Control	■	■	■
OVM-Aware Debugging	■	■	■
C Debugger	Option <sup>1</sup>	Option <sup>1</sup>	■
Memory Window	■	■	■
Multiple Waveform Windows	■	■	■
Extra Standalone Viewer	Option	Option	Option
Waveform Compare	■	■	■
Transaction Viewing and Analysis	Option <sup>1</sup>	■	■
Protocol Recognition	■	Option <sup>2</sup>	Option <sup>2</sup>
JobSpy	■	■	■
SignalSpy	■	■	■
User-Customizable GUI (via Tk)	■	■	■
<b>Simulation</b>			
Single-Kernel Simulation Engine	■	■	■
Verilog RTL & Gate Performance Optimizations	■	■	■
VHDL RTL & VITAL Performance Optimizations	■	■	■
Performance and Memory Profiler	■	■	■
Dynamic Object Capacity Profiler	■	■	■
Separate Elaboration	■	■	■
Waveform Management Tool Set	■	■	■
VCD and Extended VCD Support	■	■	■
VCD Re-Simulation	■	■	■
Batch Mode Simulation	■	■	■
Integrated Sim Farm Support (via JobSpy)	■	■	■
Interactive Simulation	■	■	■
Black Box Regression Suite Throughput	■	■	■
Checkpoint & Restore	■	■	■
SecureIP Models	■	■	■
SWIFT Interface / SmartModels	■	■	■
Synopsys Hardware Modeler Support	■	■	■
<b>Platform Support</b>			
32-Bit OS Support	Linux, Solaris, Windows XP/Vista	Linux, Solaris, Windows XP/Vista	Linux, Solaris, Windows XP/Vista
64-Bit OS Support	Linux x86-64, Solaris 64	Linux x86-64, Solaris 64	Linux x86-64, Solaris 64

<sup>1</sup> - Included in SystemC Option

<sup>2</sup> - Included with Multi-View Verification Components (MVC)