

Questa 10.0 Series Product Comparison			
Feature	Questa Core	Questa Prime	Questa Ultra
	Large Block/System Simulation and ABV	Advanced Verification, All Languages	Advanced Verification, All Languages, Fastest Closure, Low Power
General			
Licensing - Floating License	■	■	■
Language Neutral License	Option (LNL)	N/A	N/A
ASIC Sign-Off	■	■	■
Platform-Independent Compiled Database	■	■	■
Native-Compiled Architecture	■	■	■
Incremental Compilation	■	■	■
32/64-Bit Cross-Compatibility	■	■	■
Languages			
SystemVerilog IEEE1800 Design	■	■	■
SystemVerilog IEEE1800 Verification	Assertions Only	■	■
VHDL	VHDL, LNL or Mixed	■	■
Verilog	VLOG, LNL or Mixed	■	■
Mixed Language	Mixed	■	■
PSL IEEE 1850	■	■	■
Verilog PLI/VPI	■	■	■
SystemVerilog Direct Programming Interface	■	■	■
VHDL FLI	■	■	■
Unified Power Format	Option (PA Sim)	Option (PA Sim)	■
SystemC 2.2 IEEE 1666/OSCI 2.2	Option (SystemC)	■	■
Analog/Mixed Signal (Advance MS Product)	Questa ADMS	Questa ADMS	Questa ADMS
Advanced Verification			
Assertion-Based Verification	■	■	■
Questa Verification Library (Assertion Checker & Monitor Library)	Checker Library	■	■
Constrained-Random Test Generation	■	■	■
Verification Methodology Support(OVM and UVM)	■	■	■
inFact Testbench Automation	■	■	■
Power Aware Simulation and Debug	■	■	■
CodeLink (Processor-Based Verification)	■	Add On Product	Add On Product
Multi-View Verification Components (Verification IP Library)	■	Add On Product	Add On Product
Verification Management & Coverage			
Code Coverage (with Toggle Coverage)	■	■	■
Functional Coverage	■	■	■
Unified Coverage DataBase (UCDB)	Code Coverage and Assertions	■	■
Coverage Viewer	Code Coverage and Assertions	■	■
Test Ranking	Code Coverage and Assertions	■	■
Test Plan Tracking	Option (VM)	■	■
Verification Results Analysis	Option (VM)	■	■
Verification Run Management	Option (VM)	■	■
Design Entry, Debug, and Analysis			
HDL Editor	■	■	■
Integrated Project Manager	■	■	■
Source Code Templates and Wizards	■	■	■
Interactive & Post-Simulation Debug	■	■	■
Dataflow Graphical & Textual Causality Traceback	■	■	■
Schematic viewer	■	■	■
Advanced FSM Debug	■	■	■
Source Annotation	■	■	■
Hyperlinked Navigation	■	■	■
Class Browser	■	■	■
Dynamic Thread Debug & Control	■	■	■
OVM-Aware Debugging	■	■	■
Assertion Thread Viewer	■	■	■
C Debugger	Option ¹	■	■
Memory Window	■	■	■
Multiple Waveform Windows	■	■	■
Extra Standalone Viewer	Option	Option	Option
Waveform Compare	■	■	■
Transaction Viewing and Analysis	Option ¹	■	■
Protocol Recognition	■	Option ²	Option ²
JobSpy	■	■	■
SignalSpy	■	■	■
User-Customizable GUI (via Tk)	■	■	■
Simulation			
Single-Kernel Simulation Engine	■	■	■
Verilog RTL & Gate Performance Optimizations	■	■	■
VHDL RTL & VITAL Performance Optimizations	■	■	■
Performance and Memory Profiler	■	■	■
Dynamic Object Capacity Profiler	■	■	■
Simulation & Compile Flow Optimizations	■	■	■
Waveform Management Tool Set	■	■	■
VCD and Extended VCD Support	■	■	■
VCD Re-Simulation	■	■	■
Batch Mode Simulation	■	■	■
Integrated Sim Farm Support (via JobSpy)	■	■	■
Interactive Simulation	■	■	■
Checkpoint & Restore	■	■	■
VHDL 2008 Encryption	■	■	■
Verilog 2005 Encryption	■	■	■
SecureIP	■	■	■
Platform Support			
32-Bit OS Support	Linux, Solaris, Windows XP/Vista	Linux, Solaris, Windows XP/Vista	Linux, Solaris, Windows XP/Vista
64-Bit OS Support	Linux 64, Solaris 64, Win7-64	Linux 64, Solaris 64, Win7-64	Linux 64, Solaris 64, Win7-64

¹ - Included in SystemC Option

² - Included with Questa Verification IP