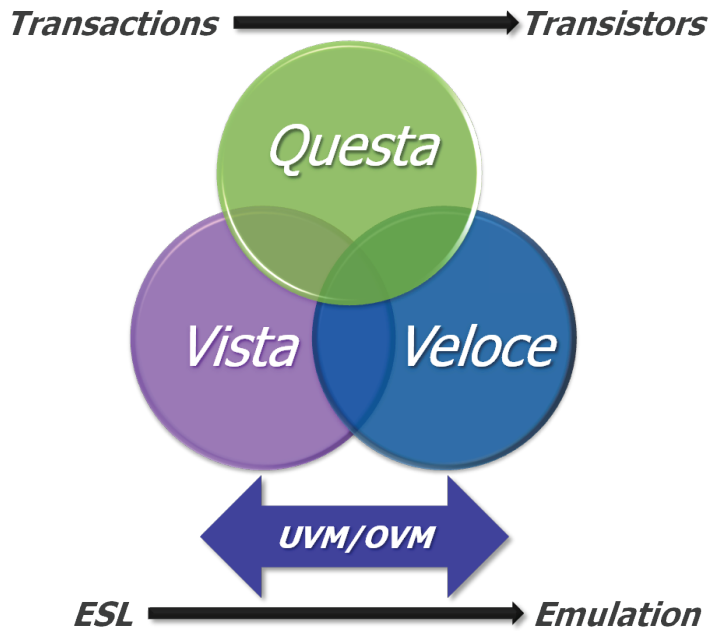


Transforming Verification Questa Verification Platform

Functional Verification

D A T A S H E E T



Mentor Graphics combines three advanced platforms, and a commitment to industry leading standards, to transform verification from transactions to transistors.

Fastest Time To Confidence

- 10X to 100X demonstrated results

Industry Leading Solutions

- Accelerated coverage closure
- Integrated verification management
- Reduced time to debug
- Low power verification
- Clock domain crossing verification

Best-In-Class Technology

- Multi-language simulator
- Formal verification
- HW/SW coverification
- UVM/OVM methodology

Transactions to Transistors, Built Upon Standards

Mentor Graphics provides three leading platforms to transform verification. At the architecture level sits Vista, a complete TLM 2.0-based solution for architecture design, analysis, verification and virtual prototyping. Vista enables system architects and SoC designers to make viable architecture decisions while allowing hardware and software engineers to validate their hardware and software. Next comes Questa, a comprehensive platform for verification complex designs. Questa is built on a core simulation and debug engine providing the industry's most complete native support of Verilog, SystemVerilog, VHDL, SystemC, PSL and UPF. And for high performance simulation acceleration and pre-silicon, real world testing using SoC in-circuit emulation, there's the Veloce product family. With up to 512 million gates and 100% internal DUT visibility, Veloce enables dramatic acceleration of block and full SoC RTL simulations and supports reuse of verification IP, including signal-level and transaction-based testbenches as well as assertion-based verification IP.

The three platforms are grounded firmly in industry leading standards, including the Universal Verification Methodology (UVM), approved by Accellera in February 2011 as a direct derivative of the Open Verification Methodology (OVM). Available as the Class Reference Manual, accompanied by an open-source SystemVerilog base class library implementation, and a User Guide, UVM establishes a methodology to improve design and verification efficiency, verification data portability, and tool and VIP interoperability.

More than a collection of best-in-class verification solutions, the Questa Verification Platform from Mentor Graphics provides the means to transform verification, from transactions to transistors, and from ESL to emulation, available today.

Introducing the Questa Verification Platform

Functional verification has evolved from gate and RTL simulation into a broader collection of verification tools. The complexity of SoCs is demanding changes in functional verification, forcing the integration of multiple point tools into flexible, open flows that integrate a broad arsenal of verification solutions. SoC verification complexity is managed by decomposing the problem and using the best solution, such as CDC verification, formal verification or mixed-signal simulation. This places tremendous importance on the verification plan and the ability to collect metrics throughout the process and across all verification tasks to track progress against the plan, allocate and manage resources efficiently, and identify trends as the project progresses against schedule.

At the same time, complexity is forcing design and verification to move up in abstraction to the transaction and algorithmic level with automated or manual refinement into an RTL implementation.

Software has become a major component of SoC system functionality, creating new requirements for block-to-system verification reuse and the need for system verification and debug. While software testing of SoC integration and basic functionality as well as the verification of low level driver software can be accomplished in simulation, long, complex sequences that exercise system functionality demand acceleration with full debug visibility.

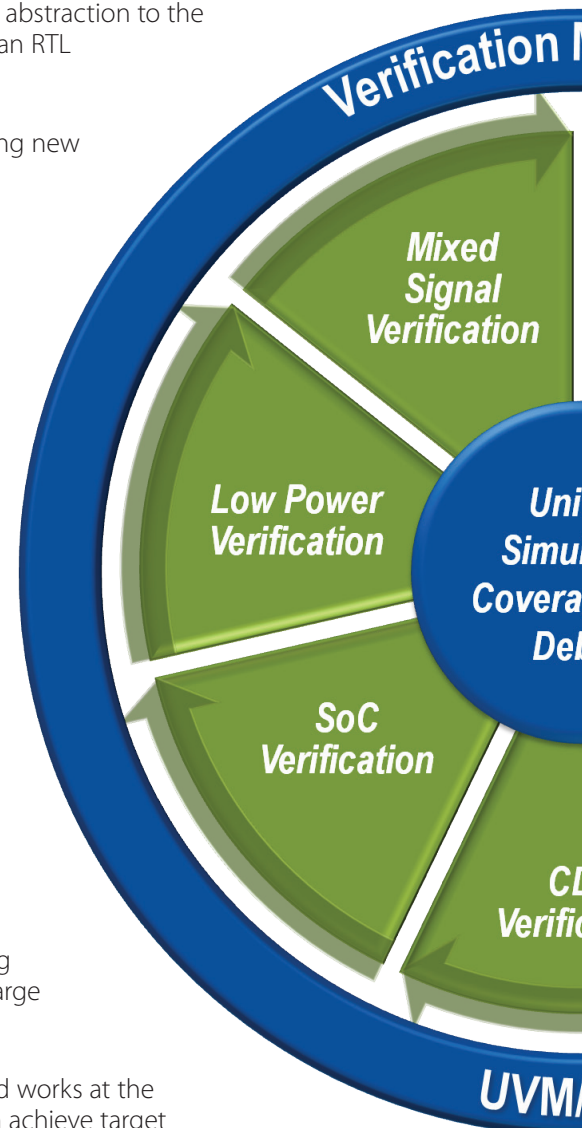
No one wants to compromise product quality. However, time-to-market pressures dominate SoC projects. To deliver quality within schedule requires improving the time to achieve coverage and quality goals.

The platform is composed of several technologies, each powerful on its own. Applied together, along with a comprehensive database and best-in-class verification management tools, the technologies deliver a powerful answer to myriad verification problems. Among these technologies:

Unified Simulation, Coverage and Debug technology, built on a best-in-class simulator. The Questa Advanced Simulator achieves industry-leading performance and capacity through very aggressive, global compile and simulation optimization algorithms for SystemVerilog and VHDL, improving SystemVerilog and mixed VHDL/SystemVerilog RTL simulation performance by up to 10X. Questa also supports very fast time to next simulation and effective library management while maintaining high performance with unique capabilities to pre-optimize and define debug visibility on a block by block basis, enabling dramatic regression throughput improvements of up to 3X when running a large suite of tests.

Intelligent Testbench Automation automatically generates sequences and works at the block, subsystem and SoC levels. The technology avoids redundancy and can achieve target coverage more than 10X faster than is possible with constrained random testing. The technology can be applied either to yield much faster runs or to allow the user to run more tests in the same amount of time — or somewhere in between — under the user's control.

Questa Verification IP provides a collection of reusable testbench building blocks that are protocol- and interface-compliant, and can be used to verify that the design implements protocols correctly. The IP, with native support for OVM and UVM, facilitates simulation, formal verification and emulation, and enables straightforward test plan tracking.



Questa CDC Verification identifies errors that have to do with clock domain crossings – signals (or groups of signals) that are generated in one clock domain and consumed in another. It does so with structural analysis and recognition of clock domains and synchronizers, and with generation of metastability models for reconvergence verification. The technology checks all potential failure modes and presents to the user familiar schematic and waveform displays.

Questa Formal Verification complements simulation. With autodetection of common errors, and support of SVA, PSL and OVL assertions, the technology provides exhaustive verification without testbenches. Its capacity and performance allow for everything from early debug before simulation tests to post-silicon debugging.

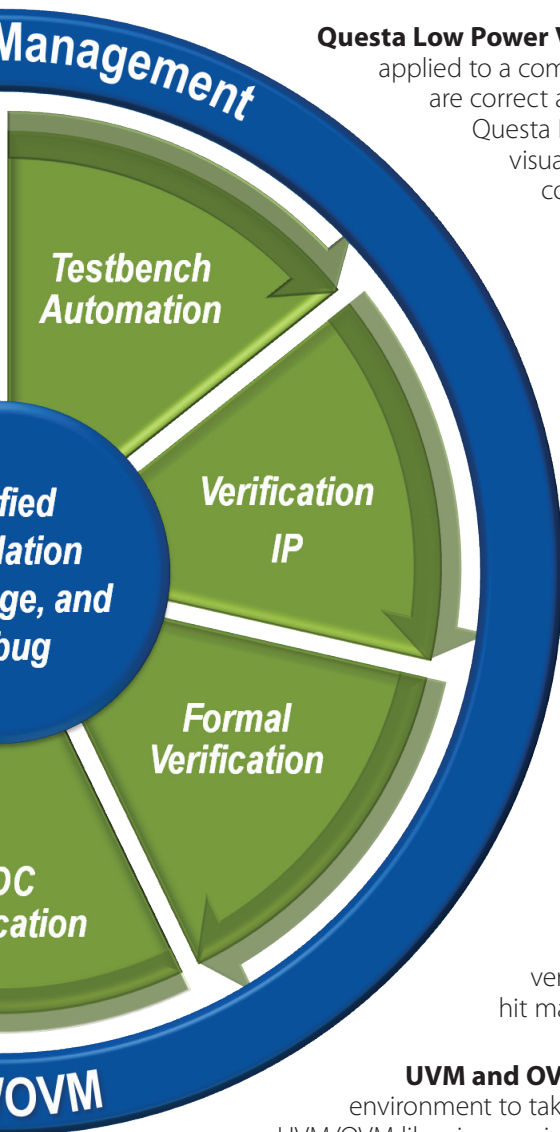
Questa Low Power Verification enables early (RTL) verification of active power management applied to a complex design, to ensure that the power management architecture and behavior are correct and that the design will operate correctly under active power management. Questa PASim simplifies the verification process through automated error detection, visualization of power management architecture and behavior, and coverage data collection for power states and state transitions. Based on industry-standard IEEE 1801-2009 UPF for specification of active power management, Questa PASim integrates well with other UPF-based tools to support multi-tool and multi-vendor design and verification flows.

Questa ADMS verifies complex analog/mixed-signal designs. The technology integrates four high performance engines: Eldo for general purpose analog, ADiT for fast transistor-level, Eldo RF for modular steady state and Questa Sim for digital. Its combination of languages and algorithms allows for both top-down design and bottom-up verification.

Questa SoC Verification provides processor-based system-level verification, using software tests to verify RTL and hardware/software integration. The technology comes with a host of advantages such as ensuring chip power management, loading and booting operating systems, and running software applications. It accelerates simulation, enables instant replay, and offers virtual emulation — all of which serve to trim debugging time.

Questa Verification Management offers a slew of features for analysis and optimization. These include the Unified Coverage Database, results and trend analysis, testplan tracking and run management. Questa Verification Management efficiently ties all coverage related tasks together and gives all parties — system architects, software engineers, designers and verification specialists — real-time visibility into the project. This visibility helps to hit market windows on schedule, manage risk and jump-start the debug process.

UVM and OVM provide a “methodology platform” so you can build your verification environment to take advantage of Questa technologies targeted to your specific application. The UVM/OVM libraries provide the infrastructure that enables you to assemble configurable VIP components and environments that can be reused from block-to-system and from project-to-project. For stimulus generation, Questa’s Intelligent Testbench Automation can be seamlessly integrated into your UVM/OVM environment. The modularity of UVM/OVM lets you reuse your transaction-level testbench using both the Questa and Veloce platforms, while also letting you gather coverage data that you can later analyze using Questa Verification Management. Questa’s unique UVM/OVM debug capabilities make it easy to debug your testbench alongside your design, too.



Verification Expertise

Mentor Graphics provides ample informational resources to help you get started adopting advanced verification techniques.

Verification Academy (www.verificationacademy.org)

The Verification Academy is organized into a collection of free online courses (modules) and resources, focusing on key aspects of advanced functional verification designed to mature an organization's verification process. Module topics include Assertion-Based Verification, FPGA Verification, Clock-Domain-Crossing Verification, Intelligent Testbench Automation and many others. Each module consists of multiple sessions allowing the viewer to pick and choose topics of interest as well as revisit topics for future reference.

The Verification Academy is the most complete UVM/OVM online resource collection. You'll find everything you need to get up to speed on UVM and OVM, whether it's downloading the kit(s) or participating in online or in-person training. The UVM/OVM modules provide a great overview of methodology concepts, introductory to advanced, with videos that walk through useful code examples. The UVM/OVM Online Methodology Cookbook is an online textbook to show you in more detail how to use the various features of the methodologies to create reusable verification components and environments.

Consulting and Training

Mentor Consulting Verification Services offers solution-driven consultants who will dramatically reduce your verification process times while improving quality. Unlike

other EDA consulting services or third party consultants, Mentor Consulting's highly experienced Verification Services team offers customized solutions and proven, structured processes to ensure projects are delivered on time and to specification, and with greater probability of first-pass success.

Mentor Graphics Education Services offers a full range of learning solutions developed specifically for electronics designers and engineers engaged in advanced verification. Users can choose the type of training that best suits their needs and schedule. These choices include unique Live Online Training, training and seminars given in Mentor Graphics training centers around the world, and on-site training and mentoring specifically designed for your company.



Questa Vanguard Program (QVP)

The Questa Vanguard Program (QVP) brings world-class product integrations and interoperability to enhance Questa verification options and

build a strong and comprehensive SystemVerilog ecosystem. QVP extends Mentor Graphics breadth of design and verification technologies through partnership with other industry leading companies that provide verification related tools and methods, verification IP, conversion services, training and consulting.

Mentor Graphics is committed to the goal of bringing transformation and measurable change to the design and verification of complex SoCs. The Questa Verification Platform with its integrated solutions and unprecedented 10x-100x results in time to confidence is the first step in delivering this transformation.

For the latest product information, call us or visit: www.mentor.com/fv

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