

Precision Physical Synthesis improves productivity by providing a single data model that simultaneously optimizes both the gate and interconnect to reduce design iterations.

Key product benefits:

- Improves productivity by combining placement with synthesis to reduce design iterations
- Easy-to-use automated physical synthesis
 - Understands physical design rules
 - Push-button optimization focuses on interconnect and gate delay
- Excellent Quality of Results
- Reduces design time by enhancing the design analysis environment
- Deterministically closes on timing
- Intuitive user interface

The Solution for Every Complex FPGA Design

In today's workplace, FPGA designers do not discuss whether or not timing closure problems are occurring, but rather how long they take to solve. In previous generations of FPGAs gate delay accounted for the majority of the total delay, but with shrinking process technologies and increasing device size and capacity, interconnect delay can exceed 70% of the total delay, requiring new approaches to achieve timing closure. Former techniques included multiple place and route runs, rewriting the RTL-code or floor-planning, but these approaches have not kept pace with technology. The productivity gap has widened as the number of design iterations has increased dramatically. The pain of multiple iterations, coupled with trial-and-error synthesis runs, as well as place and route iterations, has led to the search for better, more productive solutions.

The first to integrate physical synthesis and RTL synthesis into one unique solution, Precision® Physical Synthesis addresses the productivity and timing closure challenges caused by today's highly complex programmable devices. It combines the logical, timing, and physical worlds into a single intuitive design and analysis environment, enabling designers to take control of their design implementation and timing challenges. Precision Physical synthesis provides an RTL to placed gates solution that defines a new

approach to FPGA design, built on a single data model that simultaneously optimizes gate and interconnect delay. The result is a highly productive design environment that reduces design time by weeks and months while significantly improving performance. FPGA designers can now achieve performance and design goals quickly and predictably.

Gain Confidence in Your Design

As FPGAs continue to grow in size and complexity, time-to-market pressures leave little time for designers to also become tool experts; yet performance requirements still demand excellent results. Designers must have complete confidence in their design and synthesis tools in order to meet these challenges. Precision Physical with its highly intuitive interface, advanced FPGA synthesis technology, and sophisticated design analysis capabilities delivers correct results without lengthy iterations. Comprehensive constraints handling, coupled with state-of-the-art timing analysis, guide optimization when and where it is needed most, achieving excellent results for even the most aggressive designs. But power need not require compromising usability. Novices will quickly feel like experts using an interface that guides them step-by-step through the synthesis process and into the physical environment.

Single Environment Improves Productivity

Precision Physical covers the complete synthesis and design implementation phase of complex FPGA designs. The ability to cross-probe between the timing report, RTL source, RTL schematic and physical views allows users to identify performance bottlenecks, as well as potential functional issues in the design. Based on this information, the design can be debugged and improved quickly. Timing closure problems can be fixed by either modifying the RTL code or optimizing the cell placements - Precision Physical provides a solution that allows the user to correct either type of problem efficiently.

Taking Control to Produce a Convergent Flow

Precision Physical understands all the details of your FPGA, including device configurations, delay calculations, available resources, clocking rules and placement/packing rules. To effectively merge the logical and physical environments requires a detailed knowledge of the placement rules. Knowing where items can legally be placed reduces design iterations by making sure that the timing is achieved following place and route. But Precision Physical doesn't stop there - advanced algorithms allow you to further improve the design's performance.

Precision Physical offers you two choices to enhance the design if additional performance is needed. The automated flow is a push-button solution suitable for most designs and the PreciseView physical editing environment offers a unique and powerful solution for challenging designs that have high performance requirements.

Automated Flow

Precision Physical contains advanced RTL synthesis functionality, and enhances these capabilities with physically aware algorithms, such as placement modification, retiming, replication and re-synthesis. Precision Physical has detailed knowledge concerning the FPGA vendor design rules, and uses this data to improve quality of results by verifying that any logic or placement changes are correct. The automated flow uses this level of detail to maximize performance.

PreciseView Physical Editing Environment

Precision Physical offers designers an interactive environment called PreciseView, which complies with the vendor rules to further minimize interconnect delay. The highest performance is now achievable with the lowest possible speed grades. The PreciseView physical editing environment combines an understanding of place-

ment rules with timing analysis. Designers can mix automation and human guidance or take complete control by moving and swapping individual elements such as LUTs, registers, macros, memory blocks, etc. This intuitive design environment takes care of the low-level details and allows the user to focus on the big picture of timing closure. The ability to cross-probe between physical and logical views helps designers to quickly understand how their design is implemented on the physical device and helps them find ways to improve timing.

A designer's skill and experience can be fully utilized if you offer visibility into the implementation of the RTL design. To quickly close on timing, Precision Physical offers a direct connection between PreciseView and PreciseTime, offering interactive, incremental timing analysis.

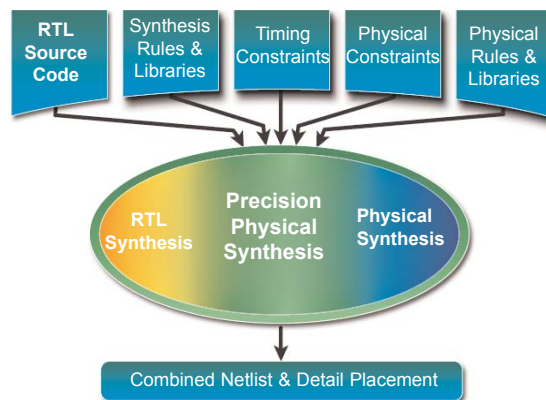
PreciseView Connects to All Views of the Design

With a single data model, Precision Physical provides a built-in set of powerful analysis features that give designers the information necessary to make important tradeoffs. These features include:

- RTL source code and schematic views
- Technology schematic view
- Physical view
- Design analysis and timing reports

About Mentor Graphics FPGA Solutions

Mentor Graphics is the market's single vendor source for an integrated solution for multi-million gate FPGA design. Our product portfolio includes best-in-class tools for design creation, simulation, synthesis, co-verification, embedded software, PCB and FPGA integration, and intellectual property. For more information visit: www.mentor.com/fpga



The Precision Physical Synthesis design environment improves productivity by bridging the gap between the logical and physical worlds.

Copyright © 2003 Mentor Graphics Corporation. Mentor Graphics and Precision are registered trademarks of their respective owners. All other trademarks mentioned in this documents are trademarks of Mentor Graphics Corporation.

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley Headquarters
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

Europe Headquarters
Mentor Graphics Corporation
Arnulfstrasse 201
80634 Munich Germany
Phone: 49-89-57096-0
Fax: 49-89-57096-4000

Pacific Rim Headquarters
Mentor Graphics (Taiwan)
Room 1603, 16F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

**Mentor
Graphics**

1022380

MM11.03