

# PADS® XE "L" ARS Suite

## PCB Design and Layout, High Speed Rules and Analysis

PADS XE "L" Suite offers superior value for a complex PCB design system with pre-layout analysis, high speed rules and reuse capabilities.

### PADS Logic

- Base schematic entry tool
- Design rule entry
- Electrical rule checking
- Cross probing with PADS Layout.

### HyperLynx® - LineSim

- Pre-layout signal integrity analysis

### PADS Layout / PADS Routers

- PCB editor
  - Online design rule checking
  - Unlimited layer manual routing
  - Library module
  - Auto-dimensioning
  - **Advanced rule setting including differential pairs**
  - Mechanical tools DXF link
  - Split-plane tool
  - **Design variants creation**
  - **Physical design reuse**
  - **4 Layer auto routing**
  - **Unlimited layer interactive routing**
  - **Unlimited database connections**
- Bold items not included in PE Suites**

### Highlights

**PADS Logic.** Basic schematic entry tool with design rule entry, electrical rule checking and cross probing of parts with PADS Layout. Very easy to use; common GUI and shared library with PADS Layout.

**HyperLynx SI Analysis.** Checks signal integrity, termination, and routing. Reviews clock topologies, board stackup. Analyzes trace lengths/effects

**PCB Editor w/ARS.** Includes manual place and route, advanced rule setting for layer, class, group, pin pair rules, and conditional levels and differential pairs; online design rule checking; auto-dimensioning, split-plane tools, a DXF link, and unlimited database connections. Design for fabrication lets you check for acid traps and starved thermals, checks, silkscreen over pads and other fabrication defects.

**RF Design.** RF design support of import of complex copper shapes, coplanar/channel Wave guide shielding, square and chamfered corners and area shielding with vias

**PADS Interactive Router.** Fast interactive route editor with unique aids for the interactive routing of length-constrained signals

**PADS AutoRouter 4L.** Shape-based autorouter with true diagonal, and any-angle routing, component fan out, pattern routing, and via optimization Routes four simultaneous layers.

**Physical Design Reuse.** Saves design costs and time by enabling replication of "golden circuits" in new designs or multiple replications of circuits in a design.

For more information please contact your local sales representative  
<http://www.mentor.com/products/pcb/pads/resellers/index.cfm>

