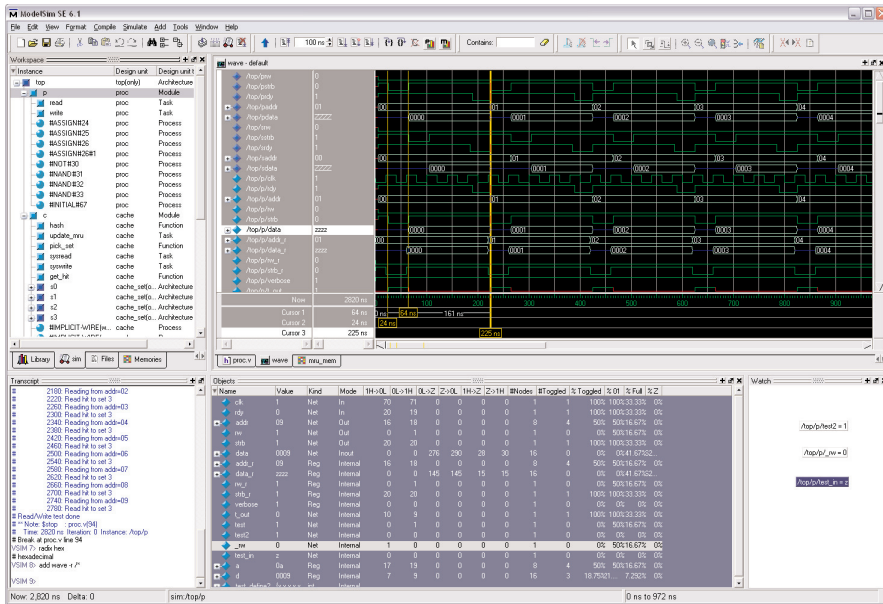


ModelSim SE



ModelSim SE is the Mentor Graphics UNIX, Linux, and Windows-based simulation environment, combining high performance with the most advanced debugging capabilities in the industry.

High-Performance Simulation Environment

ModelSim® SE combines high performance and high capacity with the most advanced verification and debugging capabilities in the industry. ModelSim SE offers unmatched flexibility by supporting 32 and 64 bit UNIX and Linux and 32 bit Windows®-based platforms. It is the cornerstone of the Mentor Graphics Scalable Verification™ solution.

Model Technology™ was the first to put the award-winning SKS technology in the hands of engineers, enabling transparent mixing of VHDL, Verilog, and SystemC in one design, using a common, intuitive graphical interface for development and debug at any level, regardless of the language.

The combination of high performance and capacity with the best integrated debug and analysis environment make ModelSim SE the simulator of choice for both ASIC and FPGA design. The best standards and platform support in the industry make it easy to adopt in the majority of process and tool flows.

Major product features:

- High-performance RTL and gate-level optimizations
- Optimized native compiled architecture
- Single kernel simulator (SKS) technology
- Tri-lingual simulator with VHDL, Verilog, and SystemC
- Powerful, intuitive GUI speeds debug and analysis of all languages
- Complete support for Verilog 2001
- SystemVerilog design
- Profiler shows both memory and CPU usage
- Advanced integrated code coverage
- Memory window
- Customizable and open architecture through C and Tcl/Tk interfaces
- Integrated JobSpy for simulation farm support
- Support for 32 and 64 bit UNIX and Linux and 32 bit Windows-based platforms

Tri-Lingual Simulator with Integrated C Debugger

ModelSim's SKS provides a unified kernel for Verilog, VHDL, and SystemC 2.1, for a true, mixed-language environment. There is no learning curve with ModelSim's SystemC implementation since SystemC code is debugged the same way as HDL code. The powerful debug environment incorporates ModelSim's exclusive built-in C debugger. Elimination of the FLI/PLI bottleneck provides both easy migration between HDL and SystemC and excellent performance. The SystemC Verification Library is also fully supported. With native support for SystemC, ModelSim offers the only authentic tri-lingual verification environment for today's complex designs.

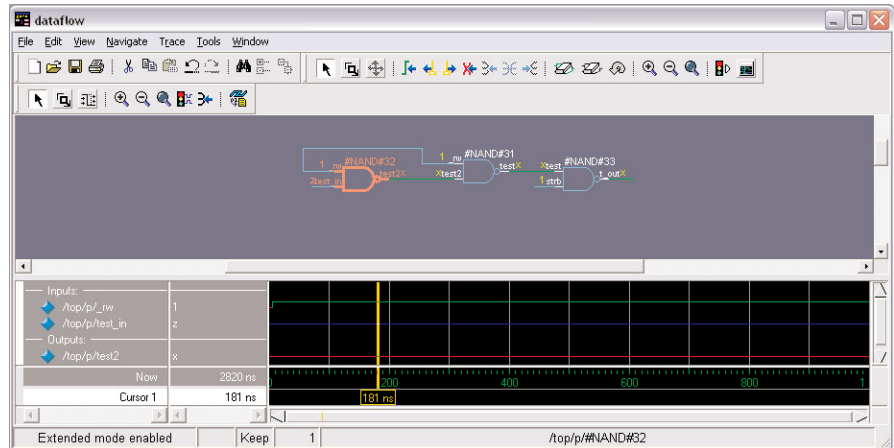
A More Intelligent GUI

An intelligently engineered GUI makes efficient use of desktop real estate. The intuitive arrangement of interactive graphical elements (windows, toolbars, menus, etc.) makes it easy to view and access the many powerful capabilities of ModelSim. The result is a feature-rich GUI that is easy to use and quickly mastered.

SystemVerilog for Design

ModelSim SE fully supports the SystemVerilog design constructs, providing new capabilities that aid in modeling at higher levels of abstraction. Some of the most significant design productivity features include:

- Interfaces
- Enumerated types
- Structures and unions
- User-defined types
- Assignment and increment/decrement operators
- Enhanced procedural blocks: *always_comb*, *always_ff*, and *always_latch*



ModelSim SE native support of SystemVerilog design constructs enables high-level design modeling and debug.

- Jump statements
- Dynamic arrays
- Associative arrays
- Direct programming interface (DPI)
- Implicit port connections: *** and *.name*
- Packages and global declaration

ModelSim's native support of SystemVerilog also includes a fully integrated debug environment.

Graphical Usage Profiler

The profiler provides an interactive graphical representation of both memory and CPU usage on a per instance basis. It shows which part of the design is consuming resources (CPU cycles or memory), allowing engineers to more quickly find problem areas in their code.

The memory allocation profiler provides insight into how much memory different parts of the design are consuming. Profiling Memory usage can be tracked during both elaboration and simulation.

Advanced Code Coverage

ModelSim's advanced code coverage capabilities are integrated into the tool. Integrated code coverage provides the highest performance with the greatest ease of use. ModelSim coverage metrics provide instance-

based results for all supported metric types. The types now supported include:

- Statement coverage: measures the number of statements executed during a run
- Branch coverage: measures the expressions and case statements that affect the control flow of the HDL execution
- Condition coverage: breaks down the condition on the branch into elements that make the result true or false
- Expression coverage: the same as condition coverage, but covers concurrent signal assignments instead of branch decisions
- Enhanced toggle coverage: in default mode, counts low-to-high and high-to-low transitions; in extended mode, counts transitions to and from X.

Please refer to the Code Coverage datasheet and application note at www.model.com for additional details on how ModelSim's advanced code coverage capabilities improve verification.

JobSpy

With integrated support of standard load sharing software, JobSpy provides the ability to easily manage and interact with simulation batch jobs. The JobSpy interface allows you to select any submitted batch job, monitor its status, or submit commands; such as, save a snapshot of a waveform, query simulation time, or suspend the job. This can be accomplished with the easy-to-use graphical interface or via the command line interface.

Memory Window

The Memory window allows flexible viewing and changing of memory locations. VHDL and Verilog memories are auto-extracted in the GUI allowing

powerful search, fill, load, and save functionality. The Memory window allows pre-loading of memories, saving the time-consuming step of initializing sections of the simulation merely to load memories. All functions are available via the command line, allowing their use in scripting.

Performance Optimization

ModelSim is proven on today's largest multimillion gate designs. ModelSim's default simulation mode delivers the industry's highest productivity debug environment. As a design matures, ModelSim's *vopt* performance mode can be enabled, thus engaging the industry's leading advanced algorithms to significantly improve simulator performance and gate-level capacity. The optional *vopt* flow automatically optimizes all Verilog and VHDL code in a design.

For regression applications and extremely large designs, ModelSim allows users to save their designs as reusable elaboration files. This improves run-time performance by eliminating the need to re-elaborate the design for each simulation run.

Complete Product Support and Maintenance

Model Technology provides the highest level of support in the industry through its unique Engineer of the Week approach. Customers receive support from the engineers who design the ModelSim products. A standard annual maintenance contract provides technical support, maintenance releases, the *Informant* email newsletter, and access to on-line support and technical services.

Visit our web site at www.model.com for the latest product news.

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Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1603, 16F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

