

ModelSim 6.5 Series Product Comparison			
Feature	ModelSim PE	ModelSim DE	ModelSim SE
	Block/Small System Simul. Windows	Block/Small System Simul. Windows/Linux	Large Block/ System Simul. All Platforms
<b>General</b>			
Licensing - Floating License Feature	Option	Option	■
Language Neutral License			Option
ASIC Sign-Off			■
HDL Editor	■	■	■
Integrated Project Manager	■	■	■
Source Code Templates and Wizards	■	■	■
Platform-Independent Compiled Database	■	■	■
Native-Compiled Architecture	■	■	■
Incremental Compilation	■	■	■
32/64-Bit Cross-Compatibility			■
<b>Languages</b>			
Either VHDL, either Verilog	■	■	■
VHDL Plus Verilog Dual Language (Mixte)	Option	Option	Option
Verilog 2001, 2005	■	■	■
SystemVerilog Design	■	■	■
SystemVerilog and PSL IEEE 1850 Assertions		■	Option (Questa)
SystemC 2.2	Option	Option	Option
Analog/Mixed Signal (Questa AMS Product)			Option
Verilog PLI/VPPI	■	■	■
SystemVerilog Direct Programming Interface	■	■	■
VHDL FLI Debug Interactive Debug			■
<b>Debug</b>			
Interactive Debug	■	■	■
Post-Simulation Debug			■
Enhanced Dataflow Window	Option	■	■
Source Annotation	Option <sup>1</sup>	■	■
Hyperlinked Navigation	■	■	■
Assertion Thread Debug		■	■
Advanced FSM Debug			■
C Debugger	Option <sup>2</sup>	Option <sup>2</sup>	■
Memory Window	■	■	■
Extra Standalone Viewer	Option	Option	Option
Multiple Waveform Windows			■
Waveform Compare	Option	■	■
Transaction Viewing (SystemC)	Option <sup>2</sup>	Option <sup>2</sup>	Option <sup>2</sup>
JobSpy			■
SignalSpy	■	■	■
User-Customizable GUI (via Tk)			■
Cross Referencing between Windows	■	■	■
<b>Coverage</b>			
Coverage Code Coverage (with Toggle Coverage)	Option	■	■
Unified Coverage DataBase (UCDB)	■*	■	■
Coverage Viewer	■*	■	■
Test Ranking	■*	■	■
HTML Reporting	■*	■	■
<b>Simulation</b>			
Single-Kernel Simulation Engine	■	■	■
Verilog RTL & Gate Performance Optimizations			■
VHDL RTL & VITAL Performance Optimizations			■
Performance and Memory Profiler	Option	Option	■
Separate Elaboration			■
Waveform Management Tool Set	■	■	■
VCD and Extended VCD Support	■	■	■
VCD Re-Simulation	■	■	■
Batch Mode Simulation	■	■	■
Integrated Sim Farm Support (via JobSpy)			■
Interactive Simulation	■	■	■
Black Box Regression Suite Throughput			■
Checkpoint & Restore			■
VHDL 2008 Encryption	■	■	■
Verilog 2005 Encryption	■	■	■
SWIFT Interface / SmartModels	Option	Option	■
SecureIP	Option <sup>3</sup>	■	■
Synopsys Hardware Modeler Support			■
<b>Platform Support</b>			
32-Bit OS Support	Windows XP/Vista	Windows XP/Vista/Linux	Linux, Solaris, Windows XP/Vista
64-Bit OS Support			Linux x86-64, Solaris 64

1 - Included in Enhanced Dataflow Option

2 - Included in SystemC Option

3 - Option for use with VHDL

\* - Data generated with code coverage opt