ModelSim and Questa Core 10.0 Series Product Comparison

Feature	ModelSim PE *Block/Small System Simulation, Windows*	ModelSim DE *Quality Critical Designs, Windows/Linux*	(no longer available for new sales) ModelSim SE *Large Block/System Simulation, All Platforms*	(part of Questa Series) Questa Core *Large Block/System Simulation, ABV All Platforms*
General				
Licensing - Floating License	Option	Option	■	■
Language Neutral License			Option (LNL)	Option (LNL)
ASIC Sign-Off			■	■
HDL Editor	■	■	■	■
Integrated Project Manager	■	■	■	■
Source Code Templates and Wizards	■	■	■	■
Platform-Independent Compiled Database	■	■	■	■
Native-Compiled Architecture	■	■	■	■
Incremental Compilation	■	■	■	■
32/64-Bit Cross-Compatability			■	■
Languages				
VHDL 1987, 1993, 2008 (partial)	■	■	■	■
Verilog 2001, 2005, 2009	■	■	■	■
VHDL/Verilog Mixed Language	Option	Option	Option (MixedHDL)	Option (MixedHDL)
SystemVerilog for Design	■	■	■	■
Assertions (PSL for VHDL or Verilog; SVA for Verilog)		■		■
Verilog PLI/VPI	■	■	■	■
SystemVerilog Direct Programming Interface	■	■	■	■
VHDL FLI			■	■
SystemC 2.2	Option	Option	Option	Option
Analog/Mixed Signal (Questa ADMS Product)			Option	Option
Debug				
Interactive Debug	■	■	■	■
Post-Simulation Debug			■	■
Enhanced Dataflow Window	Option	■	■	■
Source Annotation	Option[1]	■	■	■
Hyperlinked Navigation	■	■	■	■
Assertion Thread Viewer		■		■
Advanced FSM Debug			■	■
C Debugger	Option[2]	Option[2]	■	■
Memory Window	■	■	■	■
Extra Standalone Viewer	Option	Option	Option	Option
Multiple Waveform Windows			■	■
Waveform Compare	Option	■	■	■
Transaction Viewing (SystemC)	Option[2]	Option[2]	Option[2]	Option[2]
JobSpy			■	■
SignalSpy	■	■	■	■
User-Customizable GUI (via Tk)			■	■
Cross Referencing between Windows	■	■	■	■
Coverage				
Code Coverage (with Toggle Coverage)	Option	■	■	■
Unified Coverage DataBase (UCDB)	■[4]	■	■	■
Coverage Viewer	■[4]	■	■	■
Test Ranking	■[4]	■	■	■
HTML Reporting	■[4]	■	■	■
Simulation				
Single-Kernel Simulation Engine	■	■	■	■
Verilog RTL & Gate Performance Optimizations			■	■
VHDL RTL & VITAL Performance Optimizations			■	■
Simulation & compile flow optimizations			■	■
Performance and Memory Profiler	Option	Option	■	■
Waveform Dataset Management	■	■	■	■
VCD and Extended VCD Support	■	■	■	■
VCD Re-Simulation	■	■	■	■
Batch Mode Simulation	■	■	■	■
Integrated Sim Farm Support (via JobSpy)			■	■
Interactive Simulation	■	■	■	■
Checkpoint & Restore			■	■
VHDL 2008 Encryption	■	■	■	■
Verilog 2005 Encryption	■	■	■	■
SecureIP	■	■	■	■
Platform Support				
32-Bit OS Support	Windows XP/Vista	Windows XP/Vista/Linux	Linux, Solaris, Windows XP/Vista	Linux, Solaris, Windows XP/Vista
64-Bit OS Support			Linux x86-64, Solaris 64, Win7-64	Linux x86-64, Solaris 64, Win7-64

1 - Included in Enhanced Dataflow Option

2 - Included in SystemC Option

4 - Data generated with code coverage option

MS10.0a