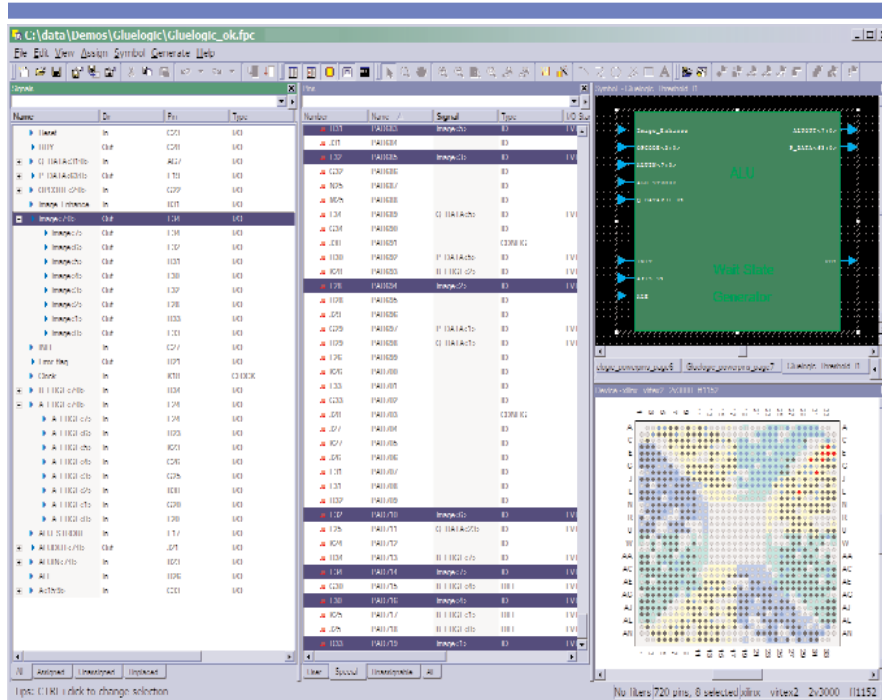


I/O Designer

The ideal focal point of advanced HDL, FPGA and PCB design

D A T A S H E E T



Major product benefits:

- Provides a graphical I/O design environment
- Serves as a bridge between your existing FPGA and PCB design flow
- Guarantees and maintains the consistency between the HDL, FPGA and PCB environments
- Supports migration to larger or smaller devices
- Automatically detects changes in HDL, FPGA Place and Route, or PCB design related files
- Provides an automated flow, thus eliminating error prone manual tasks

I/O Designer's graphical and spreadsheet based design environment.

Overview

As today's FPGA devices grow larger, so grows the difficulty in guaranteeing the consistency between FPGAs and PCBs. New devices, some offering I/O counts that exceed 1500 pins, are requiring a tool to automate the time-consuming, manual and error prone connecting of several hundred pins to the PCB. Add to that, the difficulty of swapping pins, as well as ensuring that the correct symbols, schematics, and associations for HDL designs are assigned and the amount of time necessary to create and place FPGAs increases.

To help with the growing demands of FPGA and PCB design, Mentor Graphics offers I/O Designer™, a fast and efficient solution for assigning the I/O of your FPGA to device pins. By maintaining a library of parts for Actel, Altera and Xilinx FPGAs, I/O Designer supplies all of the important information about each pin of the selected device. Using this information users can choose to assign all of the signals to pins on the device or only those signals deemed critical to the design. Users can also assign I/O standards for those signals. In this way, the FPGA pin-out can be optimised prior to PCB layout. Do you need to swap pins on the PCB to improve the layout further? I/O Designer knows which pins are swappable and which aren't.

In addition, I/O Designer manages the consistency between the FPGA and PCB flows by acting as a data management tool, monitoring each flow and managing any changes that occur. Pin swaps carried out on the PCB are picked up by I/O Designer and the necessary files updated. I/O Designer then generates FPGA place and route constraints, based on the HDL design and pin I/O assignment process, and creates the necessary symbols, schematics and hierarchical associations based on the "post-route" pin data.

I/O Designer offers a unique process for moving through the design flow, from the top level HDL description to the PCB-level symbol, as well as to the physical pin information necessary for the FPGA place and route tools. It back-annotates FPGA changes made in place and route tools, as well as in your Mentor Graphics® PCB schematic and layout tools. In addition, I/O Designer offers a central solution for the digital design engineer performing the HDL design and the physical implementation of the FPGA, as well as for the board designer using the device symbol.

To decrease design cycle time, I/O Designer allows designers to work in parallel with PCB and FPGA designs. This parallel process requires an initial layout of the board, as well as a symbol of the device. Even though the initial pin assignment is usually done in the HDL I/O, three interacting design areas may influence the final pin assignment of a device, including:

- Functional specification changes in the HDL description.
- FPGA Place and Route related changes in the pin assignment.
- Back annotation of PCB layout changes (e.g. pin swaps to facilitate a better board layout or reduce the number of layers).

I/O Designer manages the process of design changes by observing all the design related files and automatically propagates these changes in the pin assignment.

Symbols and Schematics

I/O Designer supports most industry symbol standards by offering a customizable library of pin and symbol shapes. It also offers advanced features for the importing and exporting of symbols and schematics, including the ability to export Mentor native symbols and schematics for Design Architect[®], Board Architect[™], DxDesigner[™], Design Capture[™], and DesignView[™], as well as the ability to import schematic symbols via EDIF and XML.

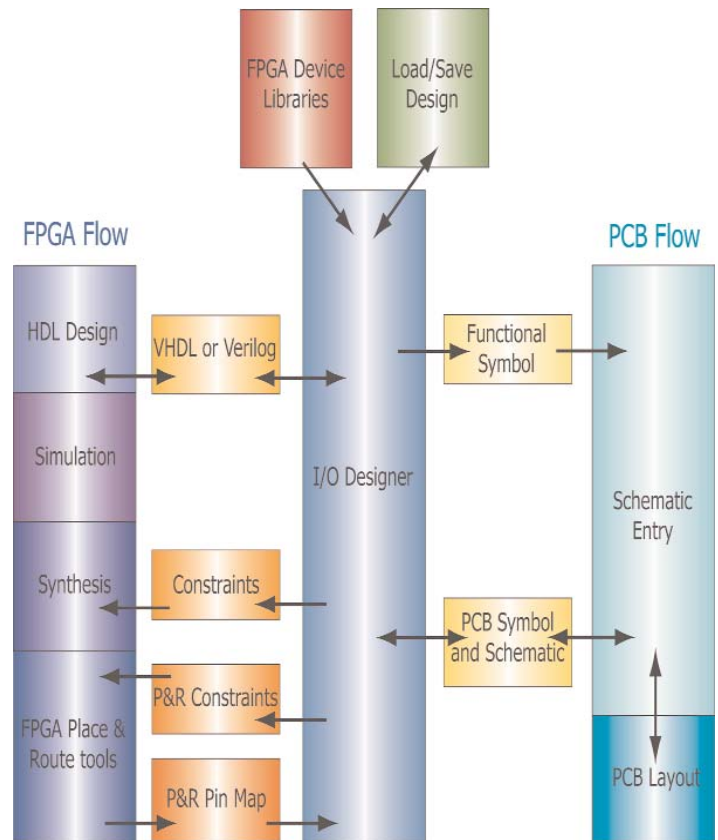
I/O Designer also provides an easy to use interface that contains a schematic symbol window that allows signals or pins to be dragged and dropped and a graphical display of footprints to map signals to pins. This interface allows for on-the-fly updates that are immediately reflected within the Mentor PCB tools and then written out to the FPGA tools.

Hardware Platforms

- PC
- Sun SPARCstation

Visit our website at www.mentor.com/pcb

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I/O Designer integrates the FPGA and PCB design flows.

Operating Systems

- Windows 2000, XP
- Solaris 2.6 or later
- RedHat Linux 7.0 or later

System Requirements

- 24 MB free disk space
- 64 MB system RAM recommended

License Configuration

- Time based
- Floating: Windows 2000, XP, Solaris, Linux
- FlexLM protected

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408.436.1500
Fax: 408.436.1501

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.40

Pacific Rim
Mentor Graphics (Taiwan)
Room 1603, 16F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886.2.87252000
Fax: 886.2.27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81.3.5488.3033
Fax: 81.3.5488.3021

Mentor Graphics



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