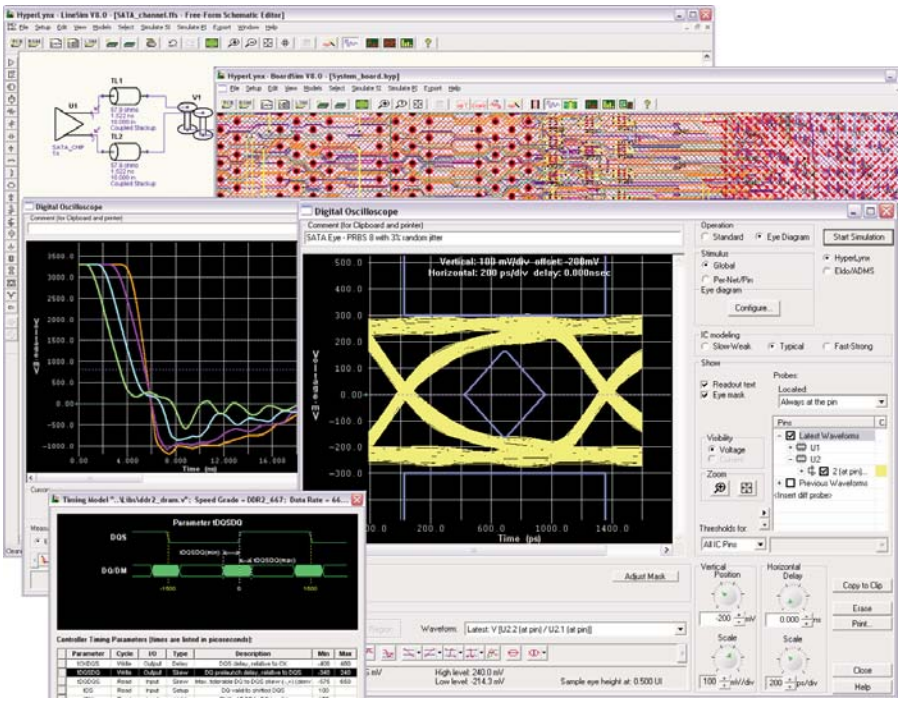
HyperLynx SI

High Speed Design

Advanced Signal Integrity Analysis

D A T A S H E E T



HyperLynx SI includes tools for pre- and post-layout signal integrity, timing, crosstalk, and EMC analysis, for signals ranging from 0 Hz to multi-GHz.

Major product features

- Industry-renowned ease of use, enabling shorter time to results
- Accurate modeling of trace impedance, coupling, and frequency-dependent losses
- Sweep different values for discretes, trace geometries and lengths, and driver settings
- Terminator wizard recommends optimal termination strategies
- Integrated timing analysis for DDR, DDR2, and DDR3
- Industry-leading SERDES support including fast eye diagram analysis, S-parameter simulation, and BER prediction
- Advanced, exploratory via modeling
- Provides an early look at likely EMC failures
- Integration with the constraint editing system
- Works with all major PCB layout and routing applications

Overview

Signal integrity (SI) analysis is an essential part of modern electronic design. Increasingly-fast edge rates in today's integrated circuits (ICs) cause detrimental high-speed effects, even in PCB designs running at low operating frequencies. As driver ICs switch faster, a growing number of boards suffer from signal degradation, including over/undershoot, ringing, glitching, crosstalk, and timing problems. When degradation becomes serious enough, the logic on a board can fail. Hardware engineers, PCB designers, and signal integrity specialists alike can use HyperLynx® as a team; getting simulation results without requiring weeks of software training. The emphasis is on getting designs right the first time, avoiding costly overdesign, and saving recurrent layout, prototype and test cycles in the lab.

Complete SI and EMC Analysis Suite

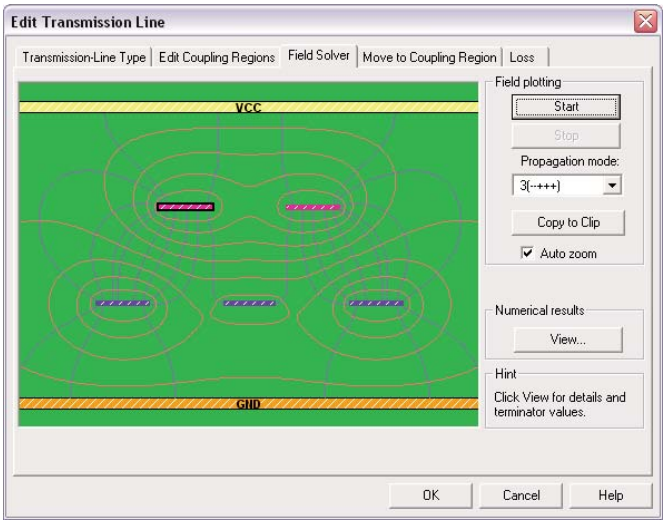
With HyperLynx, you can address high-speed PCB problems throughout the design cycle, beginning at the earliest architectural stages and moving through post-layout verification. The process is as easy as using an oscilloscope or spectrum analyzer in the lab, and at a fraction of the cost.

Mentor Graphics®

Pre-layout Analysis

Pre-layout simulation allows you to predict and eliminate signal integrity problems early. Then you can proactively constrain routing, plan stack-ups, and optimize topologies and terminations of clocks and other critical signals prior to board layout. The intuitive drag-and-drop transmission-line modeling approach is an ideal way to get your design right the first time. HyperLynx SI allows you to:

- Quickly enter complex interconnect scenarios, including ICs, transmission lines, cables, connectors, and passive components
- Simulate immediately, using industry-standard IBIS models, HyperLynx's 18,000 model IC library, generic models, or build models from databook information
- Use the Visual IBIS editor to check and edit IBIS models including a heirarchical, automated syntax
- Easily instantiate any mixture of HSPICE, ELDO, AMS, S-parameter, IBIS models.
- Start from scratch or use our many design kits for technologies like PCI Express, DDR2, and PCI-X, or one of our many FPGA design kits.
- Accurately predict serial interface bit error rates (BER), worst-case bit sequences, and eye diagrams in hours instead of weeks using HyperLynx FastEyeTM.



Pre-layout crosstalk analysis allows you to optimize spacing, stack-up, and termination.

Post-layout Verification

Post-layout verification allows you to analyze signal integrity and timing at three important stages: following part placement in your PCB layout system, after critical net routing, and after detailed routing of an entire board.

- Batch simulation automatically scans large numbers of nets on an entire PCB, flagging SI and EMC hot spots
- Interactive analysis takes you to the next level, simulating batch analysis-identified trouble spots
- Quick terminators allow new termination components to be inserted on-the-fly, enabling real-time analysis
- Accurately predicts crosstalk waveforms for any trace topology and IC placement, also showing board designers specific cross-sections in violation of crosstalk thresholds
- Powerful, easy to use multi-board analysis, including support for EBD models and connector models
- DDRx interface wizard allows complete verification of DDR, DDR2, and DDR3 memory systems, including system timing

Supported PCB Layout Systems:

- Mentor Graphics PADS® Layout, Expedition™ PCB and Board Station®
- Cadence Allegro, SPECCTRA and OrCAD Layout
- Altium Protel and P-CAD
- Intercept Pantheon
- Zuken CADStar, Visula and CR3000/5000 PWS or Board Designer

Platforms Supported

- Windows 2000/XP/Server2003, Linux RHEL 3/4/5 and SLES 9/10

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