Constraint Editor System

Reduce Costs and Accelerate Time to Market

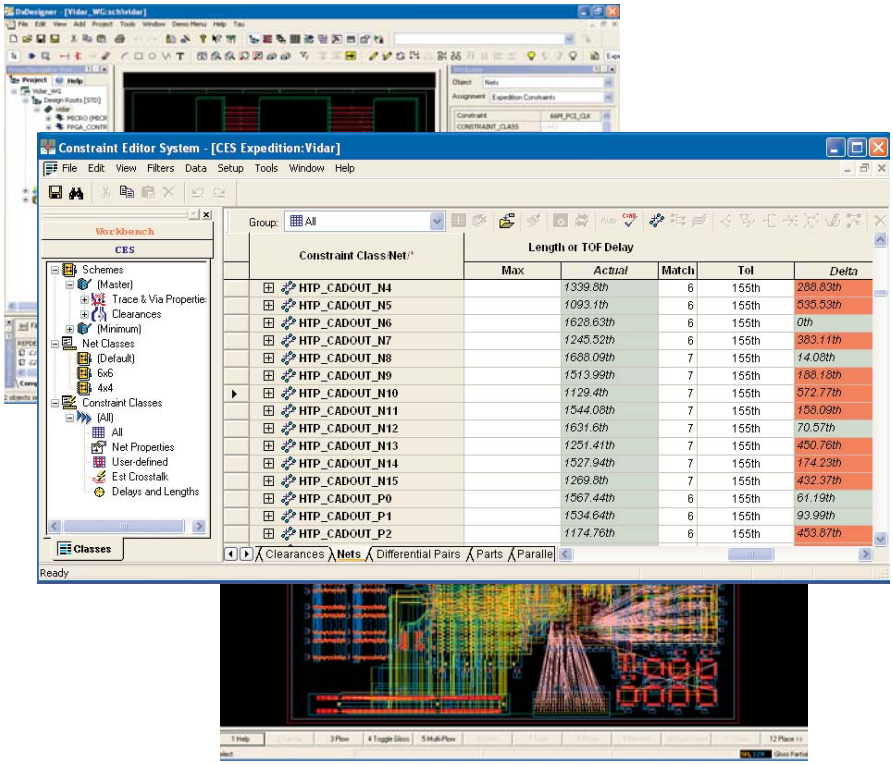

Figure 1: CES spreadsheets integrated to schematic and layout environments.

Major product benefits:

- Common constraint entry and edit for electrical and physical high-speed rules
- Integrates to all design tools from schematic to layout
- Easy-to-use spreadsheet-like GUI guided by the design database and cross probing to applications
- Rules preservation on net renames, connectivity additions/removals, pin and/or gate swaps and stackup changes
- GUI offers easy differential pair creation, parallelism rules entry and pin-pair creation
- Hierarchical constraint entry enables simple assignment of complex topologies with filtering and sorting
- Employs user-level customization and integration into the automation layer

Introduction

As designs increase in complexity and density, a higher percentage of the design must be implemented with strict adherence to design rules. Manual documentation, translation, and interpretation of design rules often cause longer product development cycles and increased costs. The Constraint Editor System (CES) provides a fully integrated, constraint-driven design methodology that reduces design costs and time-to-market by automating the communication of design rules and eliminating unnecessary PCB prototypes and re-spins. CES provides both electrical engineers and PCB designers with direct control over the most advanced routing technology in AutoActive to solve current and future system design requirements.

Constraint Integration throughout the Design Flow

CES supports bi-directional cross probing, highlighting and selection between a spreadsheet-based constraint interface and the schematic capture and physical design tools in the flow. The list of tools includes Design Architect®, Board Architect™, Board Station®, Board Station® RE, DxDesigner™ and Expedition™. Constraint values are fully synchronized during the forward and backward annotation processes with intelligent handling of connectivity changes.

Hierarchical Rule Classes

With CES, users can create hierarchical rule classes that greatly ease the association of constraints to design objects. With more common "flat" systems, users must apply constraints to many individual nets or pins, but with the use of hierarchy, and the inheritance of constraints that this facilitates, those same nets can be constrained by one rule at the class level. This greatly reduces the number of constraints manually entered in the design, so when a constraint changes, due to packaging or other requirement changes, constraint modification is simple and straightforward.

Topology Assignment

CES supports user-defined and pre-defined automatic topologies. Users can create a topology and associated constraints with user positioned virtual pins or they can use the more sophisticated automatic topologies where the AutoActive® environment intelligently manages virtual pin locations. Constraint templates can be used to copy constraints from one net to an entire bus, including custom ordering, net constraints and pin pair constraints.

Net Class Schemes

Schemes allow users to have area specific manufacturing constraints, which override the design wide or layer specific constraints. These include constraints such as widths and clearances, which may have to be modified, for example, around a Ball Grid Array device. These schemes are then mapped to rule areas in the AutoActive environment.

Differential Pair Creation

Differential pairs are becoming more and more prevalent in today's designs. CES allows users to easily assign these with a differential pair finder utility. This utility allows users to assign differential pairs using common naming conventions, wild card searches on net names and information from the interactive selection of pairs of nets across the entire design.

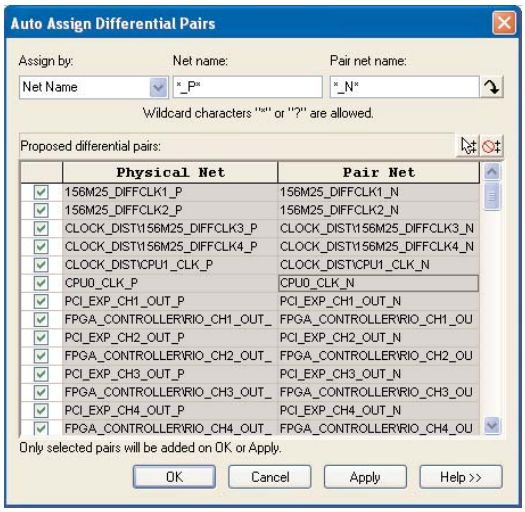

Figure 2: Identify differential pairs quickly using wildcard searches.

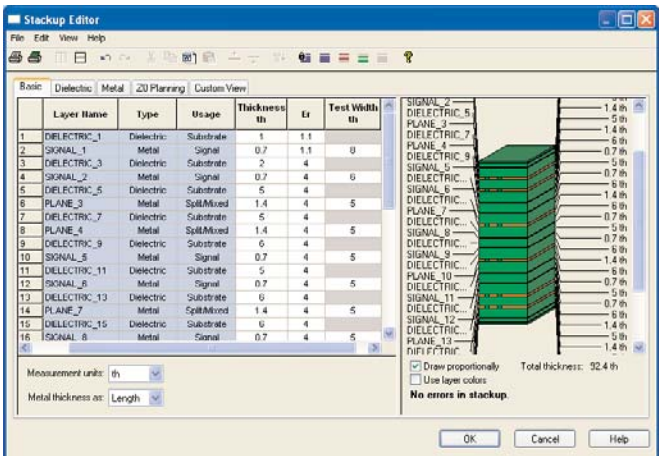

Figure 3: Graphical view of layer stackup with impedance planning.

Impedance Planning

Users have the ability to view or modify the properties of the stackup associated with a design within CES. By doing so, users can verify existing stackup characteristics such as differential pair impedance, modify layer attributes, and/or augment the stackup to meet width, spacing and impedance constraints.

Parallelism Rule Assignment

CES provides a simple parallelism rule creation and assignment dialog box. Parallelism rules apply on the same or adjacent layers and can be assigned at the net or class level for maximum control and flexibility.

System Requirements

Operating Systems:

- HP-UX: 11.0, 11i
- Red Hat Enterprise Linux: WS 3
- Solaris: 8, 9
- Windows: 2000 SP4, XP Pro SP1a

Memory:

- 512 MB Minimum
- 1GB Recommended

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