

EXPEDITION ENTERPRISE

The technology leader for today's most complex PCB systems designs

Mentor
Graphics®



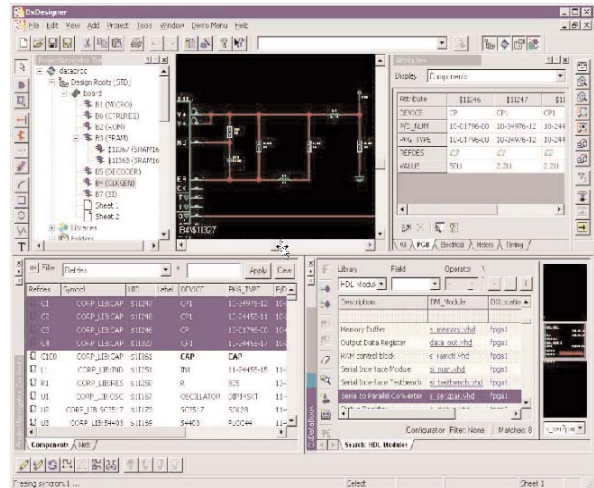
Tightly Integrated Flow

It's Expedition™ Enterprises tightly integrated design environment, industry unique technologies and its ability to meet the needs of mid-sized to large electronics companies that really sets it apart from the competition. It features a common database and user interface, with rules that eliminate the burden of managing multiple tools to complete a design. Its electrical and manufacturing constraint management system, and design data and library management provides support for local or globally dispersed design teams to leverage their resources and reduce design cycle times. Data integrity is constantly maintained — from concept to manufacturing. Expedition Enterprise is integrated with DMST™ (Data Management System) and CES (Constraint Editing System), providing a central infrastructure for component libraries, design data versioning and management, design reuse, where used, entry and management of high speed and manu-

facturing rules, and integration with corporate PLM systems. Once the design is complete, integration with manufacturing output tools ensures that the integrity of the design is maintained.

Industry-Unique Technologies

While tight integration provides a seamless environment to support the PCB systems design team, Expedition Enterprise has extended beyond the classical definition of a PCB design solution and contains many industry-unique technologies. These technologies address the most advanced business needs of an electronics company enabling the development team to deliver a more competitive product to market faster and at reduced cost. These unique technologies



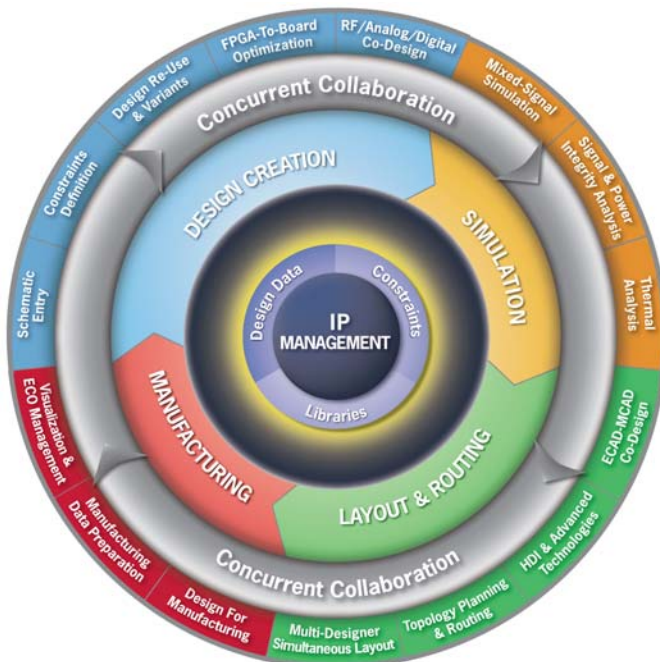
DxDesigner provides a complete solution for design creation, definition, and reuse

fall into three categories: concurrent (parallel vs. serial) product development processes; use and analysis of the most advanced IC and PCB fabrication technologies; and, collaboration between the PCB designer and other disciplines in the product development process.

System Definition

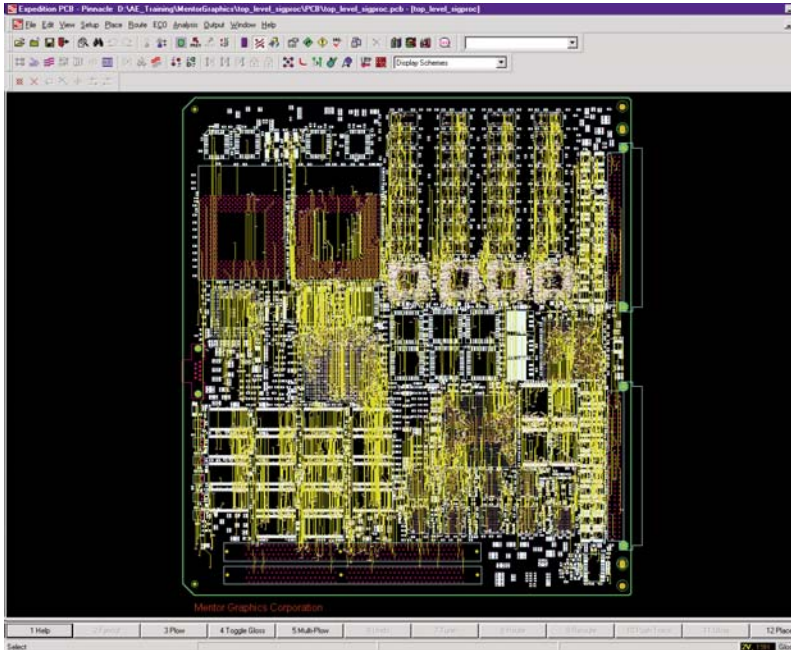
Design Entry

DxDesigner provides a complete solution for design creation, definition and reuse. It provides everything needed for circuit design and simulation, component selection and library management, signal integrity planning, project management and team-based design. With DxDesigner, multiple engineers can work on the same design concurrently without a classical split and re-join process. Changes made by one engineer are immediately reflected in the master database being viewed by the team so interfaces between the schematic sheets are kept in sync. In addition to classical schematic symbols, DxDesigner supports spreadsheet input of component and interconnect data. This is especially important to accommodate very-high-pin-count packages, where a schematic symbol would occupy several pages.



Expedition Enterprise delivers industry-unique technologies to product development

For demonstrations of Expedition Enterprise's advanced technology go to:
<http://www.mentor.com/products/pcb-system-design/multimedia/>



Expedition Enterprise is simply the most productive solution available for the creation of dense, difficult, high technology PCB designs

DxDesigner is also integrated with product lifecycle management systems, making design data, PDF schematics, and BOMs available throughout the company. It also has a centralized, Internet-based library so only one version of the corporate library needs to be maintained.

ASIC-FPGA-PCB Design Collaboration

To help with the growing demands of FPGA, ASIC, and PCB design, I/O Designer™ is a fast and efficient solution for assigning FPGA and ASIC I/O to device pins in the PCB layout. I/O Designer integrates the IC and PCB design flows to provide top-down concurrent design of the FPGA/IC packages and the PCB, reducing the design cycle time and optimizing system-level performance.

By maintaining a library of parts from major FPGA vendors, I/O Designer supplies all of the important information about each pin of the selected device. Users then choose to

assign all of the signals to pins on the device or only those signals deemed critical to the PCB design. They can also assign I/O standards for critical signals. This way, the pinout of single or multiple FPGAs can be optimized prior to PCB layout to insure the best system performance, reducing PCB routing congestion and design cycle time. Need to swap pins on the PCB to further improve the layout? I/O Designer knows which pins are swappable and which are not. I/O Designer also maintains the consistency between the FPGA and PCB flows by acting as a data management tool, monitoring each flow and managing any changes that occur. Pin swaps carried out on the PCB are picked up by I/O Designer and the necessary FPGA files updated. It then generates FPGA place and route constraints, based on the HDL design and pin I/O assignment process, and creates the necessary symbols, schematics and hierarchical associations based on the "post route" pin data.

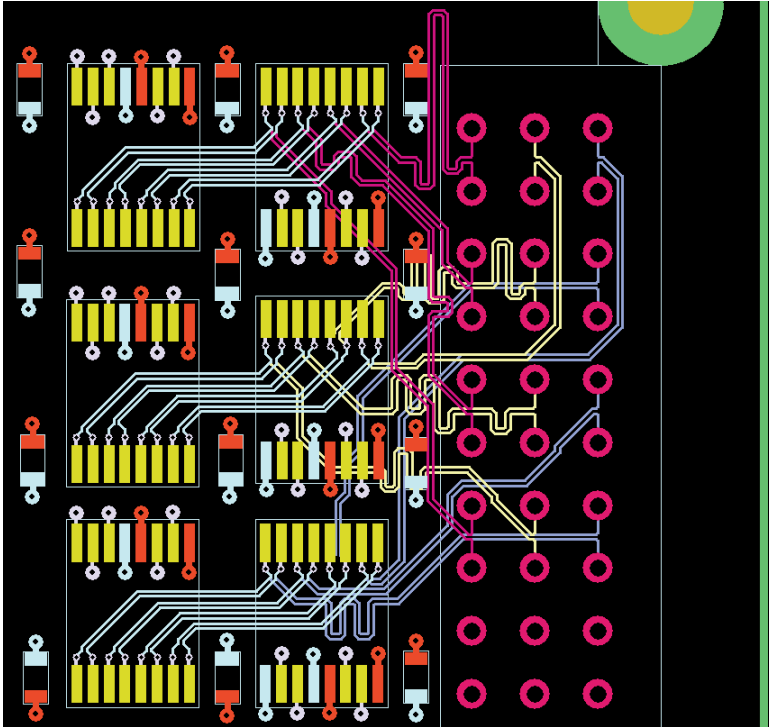
For ASIC (SoC) packages and system-in-package (SiP) designs, I/O Designer lets package designers balance IC placements, orientations, and pin assignments to optimize the design of the package and the target PCB.

Constraint Definition

Expedition Enterprise understands and follows an extensive set of high speed and manufacturing constraints (rules). These constraints are set either by engineer direct entry or by interfacing from pre-layout high speed analysis and are obeyed throughout the layout and verification steps to insure correct by design results.

The Constraint Editor System™ (CES) provides a fully integrated, constraint-driven design methodology that reduces design costs and time-to-market by automating design rules communication and eliminating unnecessary PCB prototypes and re-spins. And, like DxDesigner, multiple engineers can input and edit constraints concurrently without a divide and re-join methodology that can be error prone and time consuming. Edits are viewed by the team as they are made, in real time. CES provides common constraint entry for manufacturing and electrical and physical high-speed rules. CES has an easy-to-use spreadsheet-like GUI guided by the design database with cross probing to the schematic and layout.

- Rules are preserved on net re-names, connectivity additions/removals, pin and/or gate swaps, and stackup changes.
- The GUI offers easy differential pair creation, parallelism rules entry and pin-pair creation.
- Hierarchical constraint entry enables simple assignment of complex topologies with filtering and sorting.



Routing and editing differential pairs with Expedition PCB is accomplished with speed and ease that will change your view of high-speed design

PCB Layout

Expedition Enterprise is the most powerful physical-layout solution in the industry. By combining ease-of-use with advanced functionality, Expedition offers designers the leading technology to create today's most complex designs. It includes interactive and customizable multi-pass auto-routing controls for design challenges, such as differential pair routing, net tuning, manufacturing optimization and HDI/microvia and buildup technology.

The Physical Layout Technology Leader in PCB Design

Expedition's placement and routing technology represents a revolutionary step forward for PCB design. The power of industry-leading auto-routing

technology is combined with interactive editing capabilities to produce a single, powerful and easy-to-use design environment. This environment eliminates the burdens of jumping between tools to get the job done and managing differences between the constraints on the auto-router and on interactive editing. Expedition provides greater control than ever before, easily switching between automatic and manual editing as needed. From simple tasks, such as defining board areas, to complex procedures that involve maintaining high-speed signal conditions, all objectives are accomplished with the system and the designer working together in real time. The net result of Expedition's technology is reduced design times, increased productivity and unmatched design quality.

Auto and Interactive Routing

- A single, integrated, place-and-route editing environment that reduces total design time and increases productivity.
- All physical rules and high speed rules are maintained.
- Correct-by-construction design that produces high-quality results with clean-up time eliminated.
- Shape-based, true 45° routing.
- The most advanced auto-routing technology ever. Stop and start the auto-router at any time: all results will be correct-by-construction.
- Dynamic clean-up of traces through the reduction of segments, prevention of acute angles, and application of pad entry rules.

Dynamic Area Fills

Expedition Enterprise automatically clears area fills around traces, vias and pads as the board is edited. Dynamic area fills are so fast, it allows users to keep their area fills turned on while they are doing all necessary edits. Moving a via pushes and shoves other vias, traces and area fills and connectivity is automatically maintained.

Rules By Area

The rules-by-area function greatly improves routing around BGAs and other fine-pitched parts. Rule areas represent complete rule sets that are obeyed by online and batch DRC and in interactive and automatic routing. Rule areas may be defined by layer and can be assigned to any polygon, rectangle or circle. Trace widths and clearances automatically change when within the rule area. Designers may also change via sizes and spans in a rule area to maximize route completion.

Multi-plov with Variable Via Patterns

Expedition Enterprise's multi-plov functionality allows designers to simultaneously route multiple nets,

including differential pairs, with true 45° routing. It can even handle routing through areas of staggered pins. Traces being routed push and shove the other vias and traces and automatically clear area fills as needed. Changes can be easily made to a variety of selectable via patterns at the touch of a button, allowing enhanced flexibility for routing into dense areas of a design.

High-Speed Layout

Designers are increasingly required to manage signal quality to achieve system performance and reduce prototype iterations. High-speed design with Expedition Enterprise is an integrated part of the design environment.

Net Tuning

While routing interactively, graphic tuning aids are displayed for guidance. Nets modified out-of-tune during edits are automatically re-tuned. The hazards dialog box dynamically updates as users edit nets, providing instant feedback to their constraints.

Nets can also be tuned automati-

cally within an auto-route pass. Tuned nets are automatically maintained as the designs are completed.

Differential Pair Routing

Routing and editing differential pairs with Expedition is accomplished with speed and ease that changes the view of high-speed design. Pair spacing rules can be established by both layer and net class. If one trace is edited, the other trace in the pair automatically moves with it. Adjacent layer differential pair routing capabilities add another valuable option for routing critical signals on a dense PCB.

Dynamic Hazard Review

Design hazards are dynamically displayed and may be individually selected and colored for easy identification. When a hazard is fixed, it is dynamically removed from the hazard list.

Simultaneous Design

XtremePCB™ is a revolutionary, patented, and exciting new technology that enables multiple PCB designers, locally or globally dispersed, to simultaneously work on a single design

database over a LAN or WAN. Unlike traditional team design methodologies that employ a split-and-join approach to design collaboration, XtremePCB requires no physical partitioning and every designer sees all other client edits in real time. Because no further training or complex setup is required, designers can be brought in at any time and from anywhere to collaborate on time-critical projects, dramatically shortening design cycles. It is ideal for large, complex designs or when specialists work on their specialty within a mixed-signal environment.

Xtreme-Powered Auto-routing

The same Xtreme technology that enables simultaneous design on the same database by multiple designers enables multi-processor auto-routing. By executing the auto-routing on up to 15 processor clients on a LAN or WAN network, users can obtain up to a 10x improvement in elapsed times. For very large, highly constrained boards, this can reduce the times from days to

Setup Parameters

General | Planes | Vias | Layer Stackup | Buried Resistors & Rise Time

Via span definitions and clearances:

Layer Range	Layer 1-2	Layer 2-3	Layer 3-6	Layer 6-7	Layer 7-8
Padstack	L: VIA014BB	L: VIA018BB	L: VIA018BB	L: VIA018BB	L: VIA014BB
Capacitance (F)	.1p	.1p	.2p	.1p	.1p
Delay (ns)	.03	.03	.04	.03	.03
Grid (th)	(Default)	(Default)	(Default)	(Default)	(Default)
Buildup 1-2					
Laminate 2-3					
Laminate 3-4					
Laminate 4-5					
Laminate 5-6					
Laminate 6-7					
Buildup 7-8					

Clearances (th)

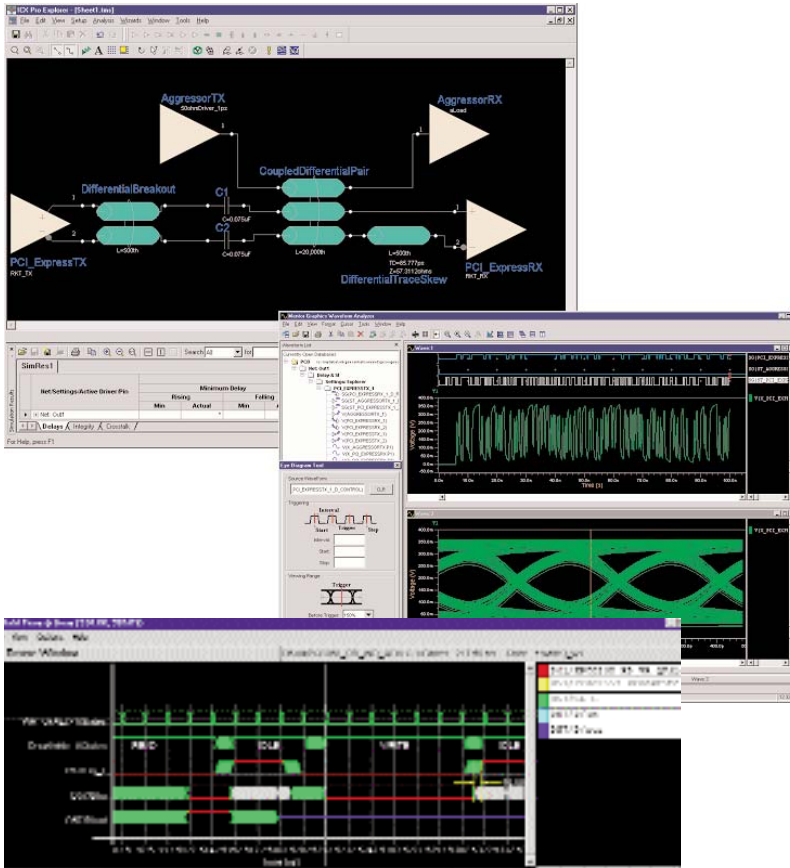
General	Layer 1-2	Layer 2-3	Layer 3-6	Layer 6-7	Layer 7-8	Through Via
Trace-Via	3	5	5	5	3	5
Via-Via 1-2	5	10	(Not Applicable)	(Not Applicable)	(Not Applicable)	10
Via-Via 2-3		5	10	(Not Applicable)	(Not Applicable)	10

Allow stacked vias by using Via Center to Via Center rules when the Same Net Clearances option is selected.

OK Cancel Apply

Expedition PCB offers the leading technology for the creation of advanced interconnect designs

For demonstrations of Expedition Enterprise's advanced technology go to:
<http://www.mentor.com/products/pcb-system-design/multimedia/>



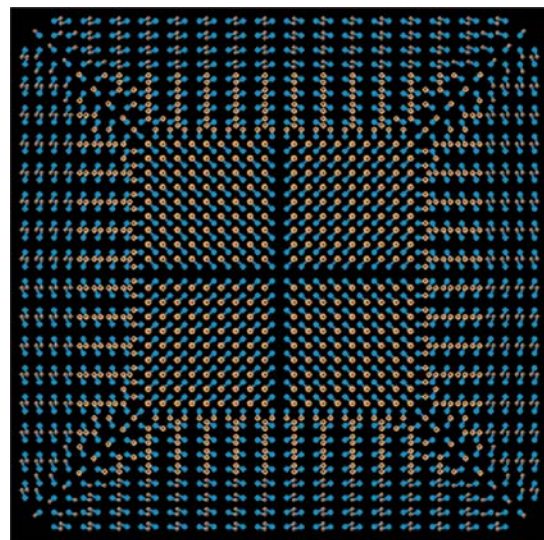
With Expedition Enterprise, timing and signal integrity issues can be addressed and corrected throughout the design process rather than just at the end

hours. The result is not only a decrease in design times but the opportunity to run multiple scenarios of placements and constraints and pick the the most cost-effective one.

Bus Routing

Auto-routing is rarely used on dense, highly bus-structured PCBs, as manual routing can produce denser, more manufacturable and aesthetic results. However, manual routing can be very time consuming and tedious. Skillful designers or engineers determine the topology of the buses and their assigned planes to meet high-speed constraints. Expedition Enterprise has unique technology that combines the skill of the designer and engineer with the speed of auto-

routing, eliminating the tedium, instead focusing on producing a better design. Topology Planner provides an interactive method of defining the topologies of buses, assigning them to planes and specifying many specialized rules. This plan is saved with the design data and can be modified. Topology Router can then be executed to auto-route the interconnects following the plan, eliminating tedious



Expedition can automatically generate a complex fanout pattern in seconds

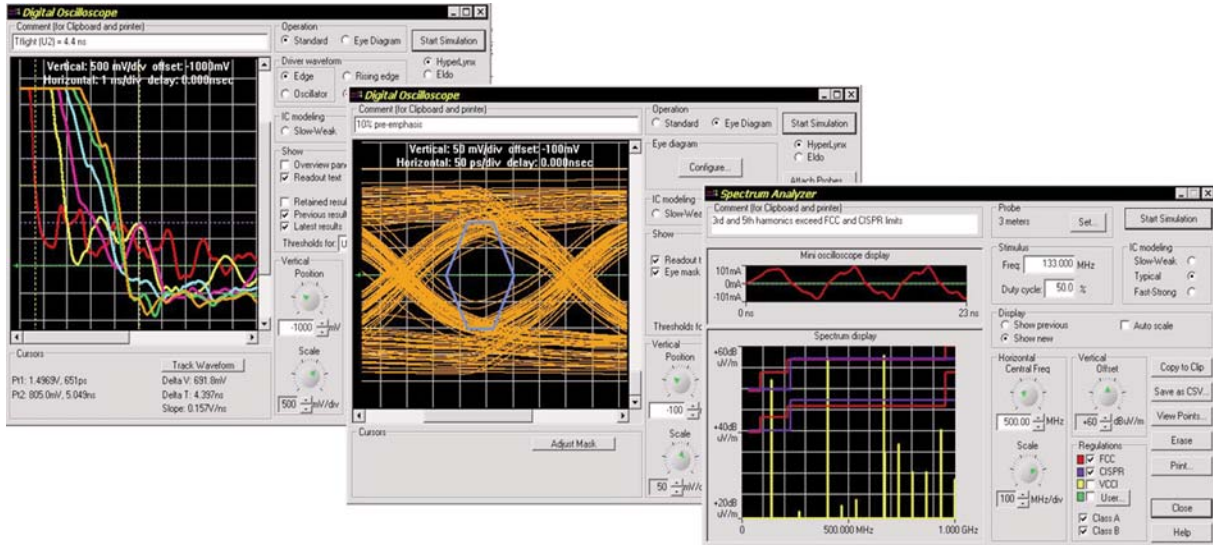
trace digitizing. The results mimic those of a skilled designer, yet significantly reduce design cycle times and improve productivity.

Embedded Passive Design

As ICs and FPGAs increase in speed and density, they require more passive components (resistors and capacitors) — some may need several hundred. Implementing these as embedded components versus discrete SMDs can significantly reduce board sizes and improve performance. Expedition Enterprise provides a complete solution: trade-off tools decide which components to implement in embedded versus discrete based on board size and cost, passive material choices, automatic synthesis driven by material supplier's libraries, and full manufacturing data generation. The result is automation of a task that could take weeks of manual effort.

Advanced Interconnect Routing

The challenges and solutions of advanced interconnect are prevalent today with BGA, CSP, COB and DCA packages increasing board density.



HyperLynx enables powerful, easy to use signal integrity, crosstalk, and EMC analysis prior to layout, after component placement, and after a board has been fully routed.

Build-up and microvia structures used in these board designs further complicate routing. Expedition PCB offers the leading technology for advanced interconnect designs, supporting the definition of complex via structure rules and the routing of microvia geometries, including routing under pads. Via spans between any two layers are possible. By moving beyond traditional laminate layer pairing, Expedition facilitates the design of build-up structures on laminate to enable escape

patterns from dense, high pin count devices. Build-up areas typically have a smaller clearance than the laminate beneath them. Expedition can establish delay values and clearances per via span to address these issues.

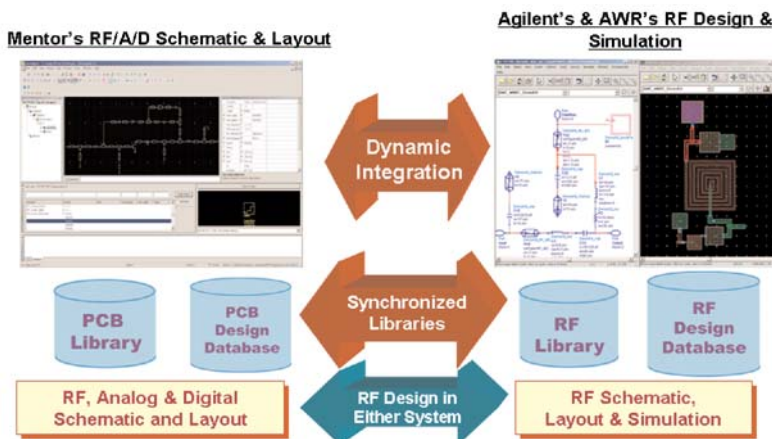
High-density BGA Fanout

Connecting to today's advanced packages can be a time consuming task for the designer. Industry unique technology in Expedition enables automatic fanout of high pin-count and

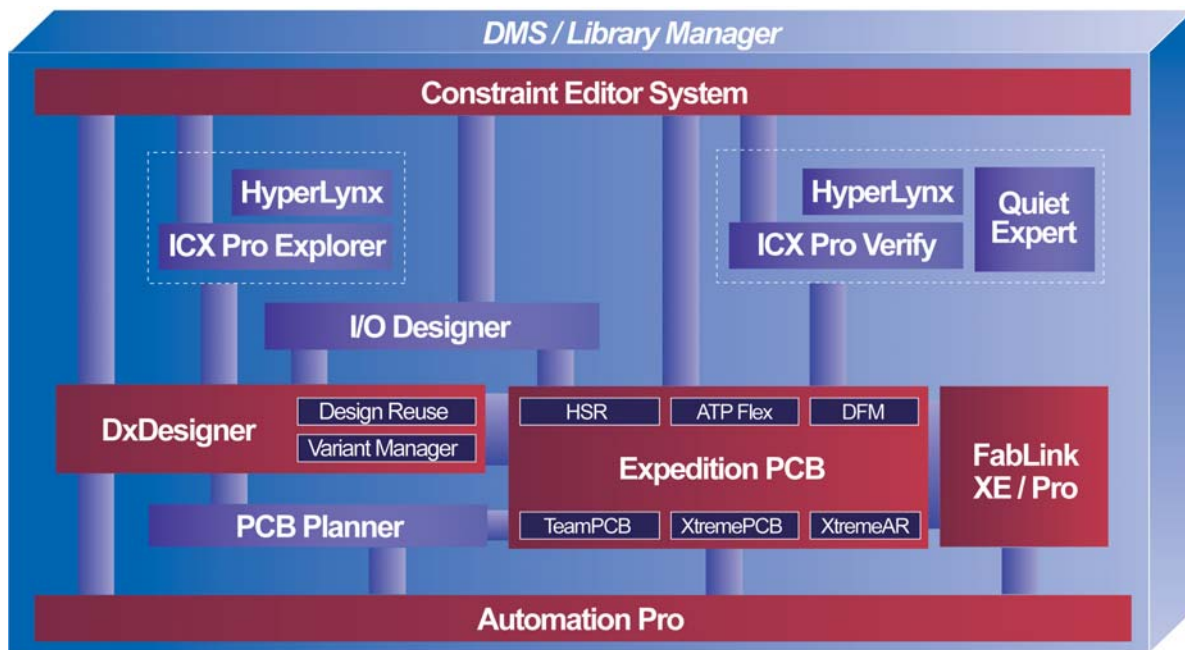
density BGAs. Following Mentor published design guidelines, the user can define the fanout pattern using HDI/microvia layers and develop the pattern in seconds. Then, in the context of the other PCB components, define and automatically produce a breakout that connects to the rest of the PCB. Reducing to minutes what used to take days of designer time.

RF Circuit Design

With the increase of wireless technology, more PCB designs mix RF circuitry with their analog and digital interconnect. Typically, designing these boards required two completely different tools and libraries. Mentor's leading technology enables RF circuit design in the Expedition Enterprise environment including schematic entry, synthesis of RF parts using the same libraries as the RF simulation providers, manipulation and editing RF circuitry, and direct interface to RF simulators from suppliers like Agilent and AWR. The result is a highly productive process that integrates the design and design team, eliminates duplication and



Expedition Enterprise enables the design and verification of digital, analog and RF on the same PCB



The Expedition Enterprise flow addresses the needs of the mid-sized to large enterprise electronics company

synchronization of libraries, and capitalizes on the strengths of Mentor's PCB design and the RF simulator suppliers' technology.

Analysis and Verification

Signal Integrity, Timing Analysis and EMI

With the Expedition Enterprise flow, signal integrity and electro-magnetic interference (EMI) issues can be addressed and corrected throughout the design process rather than just at the end. Driven by constraints in CES this ensures that designs are correct the first time, effectively reducing design iterations and facilitating optimum system performance.

HyperLynx® provides pre- and post-layout signal integrity, crosstalk and EMC analysis for traditional high-speed interconnects, as well as the emerging SERDES and DDR2/3 technologies. HyperLynx's easy-to-learn analysis environment makes it an every-desktop standard for Expedition Enterprise. Higher-frequency designs

and government regulations place increasing importance on EMI control. This normally required a prototype board, testing in a shielded chamber and re-design. Now with Quiet Expert™, the causes of EMI can be highlighted and eliminated during the design layout, thus significantly reducing design iterations and saving valuable time-to-market.

Power Integrity

With today's lower and multiple voltage ICs, power and ground is no longer easy to design and analyze. PCBs can contain as many as 30 power distribution networks jig-sawed into the PCB layers. These networks must be analyzed for DC voltage drop (sufficient power to all IC pins), current density (too much current through a narrow part of the network), and AC (is the power clean). HyperLynx PI (Power Integrity) provides the engineer and designer with pre- and post-layout analysis of complex power distribution networks to insure proper operation and high reliability of the PCB.

Thermal Analysis

As products get faster and smaller, thermal management issues increase. HyperLynx Thermal, FloTHERM®, and FloEFD® provide thermal analysis capabilities for the PCB as well as the PCB(s) in the full product (enclosure, fans, heat sinks, etc.). Using these capabilities, the PCB designer can perform analysis on the PCB to determine good placement of the components. The mechanical designer of the enclosure can insert the PCB(s) into the complete product and analyze it to see if the heat will be dissipated properly. The result is a design that has higher reliability and can be manufactured without multiple prototypes or re-spins.

Mixed Signal Verification

HyperLynx Analog™ verifies analog and mixed analog/digital designs at the system or board level. It is tightly integrated into DxDesigner and combines ease-of-use with powerful simulation, stimuli preparation, and complex circuit analysis and

verification. ModelSim® is the world's most popular and widely used VHDL and mixed-VHDL/Verilog simulator and the fastest-growing Verilog simulator.

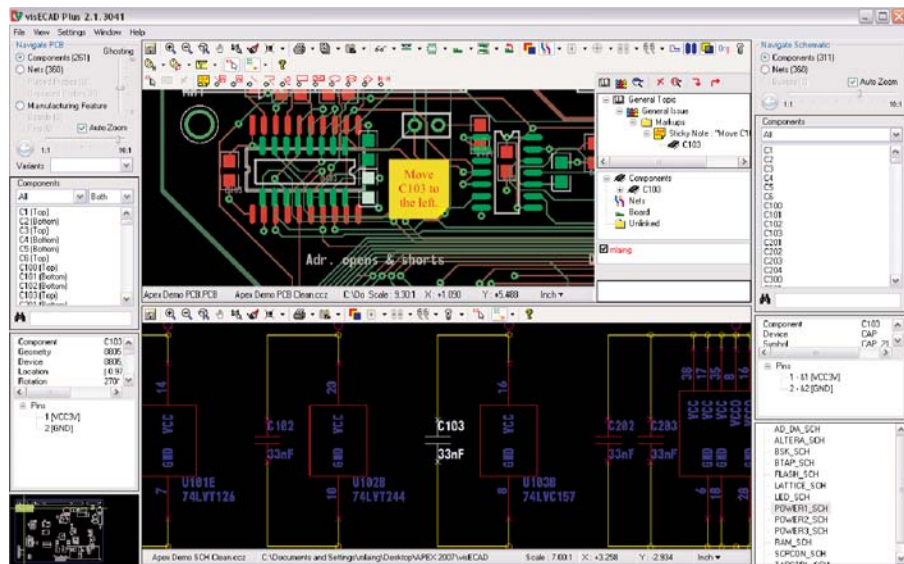
ModelSim products are unique, using technology such as Optimized Direct Compile for faster compile times and simulation performance, Single Kernel Simulation (SKS) and Tcl/Tk for greater openness and faster debugging. These exclusive ModelSim, innovations result in leading compi-ler/simulator performance, complete freedom to mix VHDL and Verilog and the unmatched customization.

Multi-disciplined Collaboration

Developing an electronic product requires more than the design of the PCB. The mechanical enclosure must be designed. Procurement, test and manufacturing must be involved throughout the design process to insure that the product can reach volume production in time to hit the market window. Expedition Enterprise provides the ability for these disciplines to collaborate during the product development process.

ECAD-MCAD Collaboration

In the past, communication between the electrical designer and the mechanical designer was performed via paper or through mass data transfers. Expedition Enterprise provides 3D viewing capability for the PCB designer to insert the PCB into the enclosure and identify gross errors such as interference of components with the enclosure. But true collaboration goes beyond 3D viewing. Expedition also provides the ability for bi-directional, electronic communica-



visECAD enables the PCB designer to electronically communicate proposed schematic and layout changes to the rest of the supply chain for their viewing and comment

tion of incremental change proposals. Using this ECAD-MCAD collaboration, either discipline can propose a change in their domain and communicate that proposal to the other. The proposal can then be analyzed, rejected, accepted, or counter-proposed. This digital process continues until both disciplines are satisfied at which point the change is reflected in both databases.

PCB Designer – Supply Chain Collaboration

Late changes in the PCB design can negatively affect the ability for procurement, manufacturing and test to deliver volume production targets. Expedition Enterprise enables the PCB designer to propose a change and electronically communicate that proposal to the rest of the supply chain organizations. visECAD™ enables these organizations to view the proposed change and communicate back to the designer through mark-ups and redlines whether this change is acceptable. This negotiation process continues until an acceptable solution is reached.

vSure DFM Verification

Concurrent DFM verification with the vSure product is the most efficient way to incorporate manufacturability into your PCB design process. Identify the opportunity for fabrication, assembly and test improvement during design, and avoid manufacturing-initiated Engineering Changes. You can even automate the intervals for DFM verification and review results in a timely manner so the design flow is streamlined and efficient. If an error is identified, a single click takes you to the location on your PCB design so that you can remedy the issue.

Comprehensive Analysis

Your DFM process is only as good as the verification tools you use. Today's miniaturized, high-layer count designs cannot be reliably reviewed by manual means. Mentor's vSure DFM verification software analyzes your PCB design with more than:

- 275 Fabrication checks
- 250 Assembly checks
- 100 Advanced Substrate checks
- 40 Microvia checks
- 30 Panel checks

In addition, vSure also provides the ability to check your Netlist against the design data to assure there are no fatal errors within this critical step. vSure validates that your BOM matches the design, and that all components in your Approved Vendors List (AVL) are an acceptable physical match.

Design Center Customization

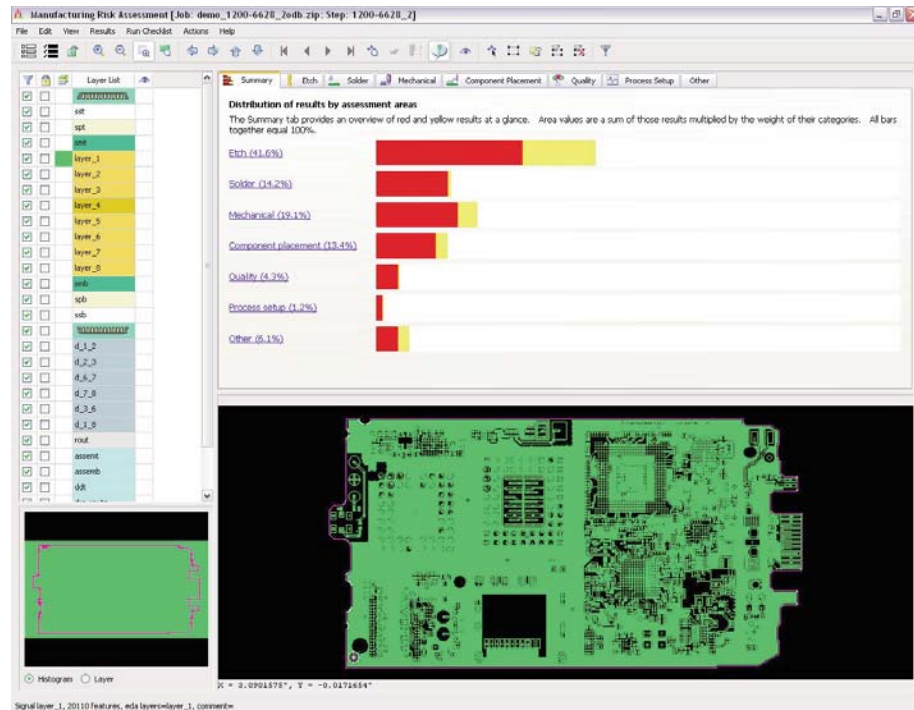
Every design center and every technology type have their own unique requirements with respect to manufacturability.

From data attribution to manufacturing rules values, you need to be able to run DFM at the highest level of automation. vSure uses a Design Center concept to allow customization of the DFM process flow, attribute mapping, component classification, and, the set-up and management of manufacturing rules files. Using a hierarchical approach, you create a master rules model using constants and variables that drive derivative rules models. This greatly reduces the support requirements for your DFM environment.

vSure even provides a default master set compliant with the IPC-7351 standard.

Understand the Manufacturing Risk

vSure not only identifies where your PCB design is in hard violation of your supplier's manufacturing capabilities, it also shows where yield or field failure issues may occur by using color severity indicators of red, yellow, and green. vSure further categorizes and prioritizes the issues so



DFM issues are summarized and ranked by severity based on userweighting

that you may easily resolve the most critical first. The weight assigned to each check is user-definable, enabling you to apply criteria to how the results are prioritized. After all, your technology and suppliers' processes are likely different than another company's processes.

FabLink XE for Fabrication

Manufacturing and fabrication have always been an integral part of PCB design. Previously, designers used multiple applications to create schematics, layouts and prepare for manufacturing. To make the process easier, Expedition Enterprise integrates the FabLink XE™ environment for manufacturing data creation, generation and verification. FabLink XE enables designers to control their fabrication data at either the board or panel level, ensuring design and manufacturing data integrity.

FabLink XE provides a standalone panel creation and editing environment for creating manufacturing data at the panel level, using a panel design database. It also provides additional board level functionality, including detailed data views, searchable PDF output, copper balancing, data outputs and Gerber In/Drill In capabilities.

Automation

Automation provides customization and extensibility within the design and layout products, allowing the addition of custom functionality, the automation of repetitive tasks, and the ability to tailor the flow to customer-specific use-cases and optimize the flow for specialized processes. The use of a wide range of industry-standard languages (VBscript, Jscript, TCL, Java, VB6, C++, C#, VB.NET...) minimizes the start-up time for company

programmers and facilitates script reuse. The result of automation is to reduce errors, increase productivity, increase the performance, quality, and reliability of the design, decrease the cost of the design, and decrease time to market (and time to profit).

Intellectual Property Management

DMS brings the electronic design process to the supply chain, and brings the supply chain to the designer's desktop. It ensures complete data consistency, accuracy and availability throughout the design enterprise. Plus, DMS consolidates multiple data systems, enabling collaboration and life cycle management across multiple team members, disciplines and sites.

It does this by integrating design data management with component information so that corporate component procurement policies (approved parts, preferred vendors) are easily available on the desktop. This helps designers make optimum component choices and manage parts lists during the design process so they can be released as accurate BOM's meeting corporate policies for cost, reliability and regulatory compliance. At the end of the project,

DMS manages the process so that accurate product documentation can be released to enterprise manufacturing, PLM and ERP systems, and supply chain management systems.

Design Reuse

The Design Reuse module creates and stores reusable blocks of circuitry, including schematic, as well as PCB placement and routing data, in a central library. These blocks can then be placed and modified in the same design or multiple designs now and in the future. Design reuse automates this process and manages the design data to ensure error-free databases and reduce the overall PCB design cycle time by not having to re-design the same circuit. Layout data can also be easily cut/pasted within a design and into other designs, enabling informal reuse of sections of a design.

Variant Management

Variant Manager manages the creation of multiple product configurations from a single design database. Variant Manager's single-point ECO management minimizes errors, reduces costs, improves design quality and enhances production efficiency.

Support, Education and Consulting

Mentor Graphics offers a full range of services to drive your productivity and success with the Expedition Enterprise flow tools. Customer Support offers award-winning technical assistance, innovative electronic support and high-quality product enhancements. Education Services offers classroom and online training to help you assimilate new tools and technologies into your design environment. Finally, Mentor Consulting is always ready to provide focused expertise in tough design areas.

Hardware Requirements

- Dual core, 2 GHz or faster
- Memory: 2 GB RAM

OS Requirements

- Windows XP Professional
- Windows 7
- HP-UX
- Sun OS
- RedHat Linux



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